Old Dominion University

ODU Digital Commons

Electrical & Computer Engineering Theses & Dissertations

Electrical & Computer Engineering

Spring 2017

A Study of the Sensitivity of Energy Conversion Efficiency to Load Variation in Class-E Resonant Power Inverter

Richard Samuel Jennings
Old Dominion University, rjennings055@gmail.com

A STUDY OF THE SENSITIVITY OF ENERGY CONVERSION EFFICIENCY TO LOAD VARIATION IN CLASS-E RESONANT POWER INVERTER

by

Richard Samuel Jennings
B.S. December 2012, West Virginia University

A Thesis Submited to the Faculty of
Old Dominion University in Partial Fulfillment of the
Requirements for the Degree of

MASTER OF SCIENCE

ELECTRICAL AND COMPUTER ENGINEERING

OLD DOMINION UNIVERSITY
May 2017

Approved by:

Yucheng Zhang (Director)

Isaac Flory (Member)

Shu Xiao (Member)

ABSTRACT

A STUDY OF THE SENSITIVITY OF ENERGY CONVERSION EFFICIENCY TO LOAD
VARIATION IN CLASS-E RESONANT POWER INVERTER

Richard Samuel Jennings
Old Dominion University, 2017
Director: Dr. Yucheng Zhang

In this thesis the sensitivity of energy conversion efficiency (ECE) and output power of a class-E resonant inverter under variable resistive and inductive load assignments is examined for wireless power transfer (WPT) applications. By performing simulation and mathematical analysis, it was found that the on-resistance of the switching device has minor effect on the design's efficiency. Additional comparisons between the simulation and mathematical analysis show reasonable output power and ECE load variation performance for the design, but with unique load impedances where zero voltage switching (ZVS) and zero derivative switching (ZDS) are achieved. These comparisons also expose inaccurate mathematical assumptions. Experimental test results are presented to validate simulation and mathematical assumptions. These tests also show invalid assumptions used in the simulation and mathematical analysis and the performance of the class-E resonant power inverter suffer due to the difference in resonant frequencies during switch on and off state periods, nonlinear shunt capacitance, and parasitic impedances.

ACKNOWLEDGEMENTS

NOMENCLATURE

C	Capacitance of resonant tank
C_1	Shunt capacitance
D	Duty cycle of Q_1
D_1	Equals (1-D) used for simplifying mathematic notation
ECE	Energy conversion efficiency
EV	Electric vehicle
$f_{r,A}$	Resonant frequency defined in circuit loop A (Figure 2) during on and off states of Q_1
$f_{r,B}$	Resonant frequency defined in circuit loop B (Figure 3) during on and off states of Q_1
$f_{r,Con}$	Resonant frequency defined in circuit loop C (Figure 4) during on-state of Q_1
$f_{r,Coff}$	Resonant frequency defined in circuit loop C (Figure 4) during off-state of Q_1
f_{SW}	Switching frequency of Q_1
GaN	Gallium-nitride
I_{DD}	Supply current amplitude
IGBT	Insulated bipolar transistor
I_O	Amplitude of output current
$I_{O,RMS}$	RMS of output current
i_O	Load current waveform
i_S	Current through C_1 during the off-state of Q_1 and through Q_1 during the on-state of Q_1
KCL	Kirchhoff's current law

KVL   Kirchhoff's voltage law

L_F Choke Inductor

L_1 Load inductance

L   Inductance of resonant tank

MOSFET   Metal oxide semiconductor field-effect transistor

PCB   Printed circuit board

PF   Power factor

P_O Active power on load

PWM   Pulse width modulation

Q_L Quality factor of resonant tank

Q_1 Switching MOSFET

R   Load resistance

$R_{DS(on)}$ On-resistance of Q_1

RMS   Root mean square

Si   Silicon

SiC   Silicon-carbide

V_{DD} Voltage of DC supply

V_{DS} Drain-source voltage of MOSFET

V_S Voltage across switch Q_1

V_O Output voltage amplitude

$V_{O,RMS}$ Output voltage RMS

X   Reactance of resonant tank

WPT   Wireless power transfer

Z	Load impedance
ZDS	Zero-derivative switching of Q_1 at turn-on
Z_{OPT}	Optimum load impedance when both ZVS and ZDS are realized on Q_1
ZVS	Zero-voltage switching of Q_1 at turn-on
Φ	Phase difference between load voltage and load current
ω	Angular switching frequency (rad/sec)

TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

CHAPTER 1

INTRODUCTION

1.1 APPLICATION DETAILS

Electric vehicles are increasing in popularity due to their affordability and renewable energy efforts. Infrastructure is required for charging the batteries of these vehicles. Traditionally electric vehicle (EV) battery charging has been accomplished by establishing an electrical cable connection between the charger infrastructure and vehicle. User inconvenience and the required maintenance associated with EV charging raise concerns with this approach due to the frequency of when these vehicles need charged. This has sparked interest in the use of wireless power transfer (WPT) technologies to allow battery charging during vehicle movement or parking without cable connections between charging infrastructure and vehicle.

Traditional EV charging systems will always be more efficient than WPT systems because of air conductivity properties. In order for the interest of WPT systems to be realized in the consumer market, the benefits of WPT must outweigh the disadvantage of the added inefficiency and the efficiency of market available WPT systems must increase. Notable state of the art WPT systems, outlined below, show promise of this aspect but opportunity for improvement is available. The transmitter topologies used in these systems are noted when known to provide consideration on the design trade-offs between transmission frequency and power switching losses of the transmitter circuit.

- A 12 kW, 22 kHz, 95.136 percent DC-to-DC efficient WPT system was integrated into a Toyota RAV4 by researchers from the Oak Ridge National Laboratory. A full-bridge inverter was used to create the transmission signal using SiC DMOS power devices. The

transmission efficiency of this system was 98.599 percent [1].

- A 3.3 kW, 19.5 kHz, 87 percent DC-to-DC efficient WPT system, called the PLUGLESS^{TM} Level 2 EV Charging System, was manufactured by Evatran Group Incorporated for charging the Chevrolet Volt and the Nissan LEAF.

- A 50 kW, 85 kHz, 95.8 percent DC-to-DC efficient WPT system was established by researchers Roman Bosshard and Johann Kolar. A full-bridge inverter was used to create the transmission signal using 1.2 kV SiC MOSFET power devices. The transmission efficiency of this system was 98 percent [2].

- A simulated 5 W, 5 MHz, 30 cm coil distance, 65.9 percent DC-to-DC efficient WPT system was established and documented in simulation results in. A class-E resonant inverter was used to create the transmission signal using power MOSFETs [3].

- A 295 W, 134 kHz, 75.7 percent DC-to-DC efficient WPT system. A class-E resonant inverter was used to create the transmission signal using HEXFET power MOSFETs [4].

In addition to air coupling power losses, WPT power system losses are comprised of passive materials of the transmitter and receiver coils and the associated power electronics for sending and receiving power in a useful manner. Increasing the transmission frequency is the most viable method to decrease total system power losses by increasing the concentration of magnetic flux lines between the transceiver and receiver. However, there is a limit to which increased design switching frequency causes other prohibitive parasitic effects and associated power losses in the power electronics and core materials [2]. This is shown in the mentioned state of art work with 85 kHz as the limit which was achieved using a full-bridge inverter. Researchers who published [3] and [4] selected the class-E resonant inverter topology for

transmitter research above 85 kHz because of its capability to operate with zero voltage and zero derivative switching to achieve higher efficiency than full-bridge inverter and other available topologies. The associated results of their research showed that the parasitic effects at higher frequency cause poorer WPT system efficiency compared to work in [2] and the need for additional research. The focus of this research begins with identifying or confirming the class-E resonant inverter as the most effective circuit topology that may be used in WPT high frequency transmitter applications.

Resonant inverters are the best suited for high frequency transmitter WPT applications because they offer relatively high efficiency and power density by operating at high frequency with zero voltage switching (ZVS) and zero derivative switching (ZDS) when compared to traditional inverters. ZVS and ZDS conditions can drastically reduce power switching losses by only changing a switch state when the voltage drop equals zero (ZVS) and with no rate of change (ZDS). A major constraint resonant inverters have is maintaining their ZVS and ZDS performance during load variation. Modern WPT systems must perform well during these conditions for varying the EV charge rate in an electric grid demand response event. Even slight load variation of these topologies from their optimum designed load impedances will degrade several key factors in system performance, such as the output active power and the energy conversion efficiency (ECE).

One method to reduce the negative effects of load variation is to utilize resonant circuit topologies with fewer switching devices, such as the class-E resonant inverter and its derivative topologies, for transmitter applications. The class-E resonant inverter offers up to 2.847 times more the output power capability of the popular class-D resonant inverter when using the same supply voltage but with up to 3.562 times higher breakdown voltage [4]. Also, the class-E

topology has one less switch than the class-D topology which is ideal to avoid poor load variation performance. The class-E topology has been known for decades and been limited from use because of the lack of feasible semiconductors to handle higher imposed voltage stress caused by fewer switching devices. However, the performance of semiconductors has greatly improved over the recent decades opening new possibilities. In addition, ongoing research and development in gallium nitride (GaN) and silicon carbide (SiC) materials offers promise to further improve power semiconductor temperature, efficiency and voltage breakdown performance [5], [6].

The class-E resonant inverter was first invented by Alan D. Sokal in 1975 for a high-efficiency, single switch RF power amplifier [7]. It achieves high-efficiency (e.g., 96 percent) by using a single switching device capable of high voltage stress and soft switching [8]. In addition to RF power amplifier applications, this topology is used in applications such as high-frequency electronic lamp ballasts [9], [10], cellular telecommunications [11], plasma heating [12], DC-DC converter [13], high-power-factor [14], microwave power [15], induction heating [16], implant electronic instruments [16] and WPT [4], [17]. In 1989, Marian K. Kazimierczuk and Jacek J. Jozwik studied the relationship between the relative bandwidth and load resistance for a class-E resonant inverter. The outcome of this work was the introduction of the class-E^2 topology which included a class-E rectifier on the load side of the class-E topology [18]. The class-E^2 topology has recently been applied to wireless power transfer applications using SiC and GaN switching devices [19]. The class-Φ and class-$\Phi 2$ topologies were also derived from the class-E topology and involve a single power switch. They were developed to maintain low voltage stress on components, provide small passive energy storage and to improve system efficiency, reliability and power density. Applications for the class-Φ and class-$\Phi 2$ topologies include electric vehicles, energy harvesting, and modern telecommunication power systems [20], [21], [22].

Similar to other resonant power inverters and converters, the output power and ECE of the class-E resonant inverter and its derivative topologies are still strongly affected by load assignment. Previous research on these topologies have provided equations for calculating the output active power and the ECE within and outside of nominal conditions [16], [23], [24], [25] and performed design and analysis for an optimum load assignment achieving soft switching [15], [26], [27], [28]. However, the previous known research only shows the power and ECE sensitivity of a specific design to variable load assignments operating with less than five watts [25]. Understanding these sensitivities at higher output power designs is important to understand the flaws of existing analytical design procedures, to better understand parasitic and nonlinear effects caused by high frequency switching operation, and to aid in producing better circuit designs and optimal control in the class-E topologies.

1.2 THESIS OBJECTIVES

Class-E resonant inverters used in WPT transmitter applications have proven to contribute to a less efficient overall system than WPT applications employing full bridge inverters. However, the class-E resonant inverter shows promise of replacing the full bridge inverter in WPT applications to improve overall system efficiency. The aim of this research is to provide contributions to a realizable, compact and efficient class-E resonant inverter that could be used in WPT transmitter applications. This will be accomplished by describing the class-E resonant inverter in Chapter 2, introducing a class-E resonant inverter design in Chapter 3, and simulationally, mathematically, and experimentally analyzing its ECE and output power sensitivity to load variation in Chapters 4, 5 and 6, respectively. The design specifications include 208 V_{DC} input voltage, 1 MHz switching frequency, and 150 W power output. Notably, the switching frequency of 1 MHz is chosen to push the limits of existing work that has been performed in this area. Chapter 7 will provide the conclusion of this work and recommendations for future work.

CHAPTER 2

DESCRIPTION OF THE CLASS-E RESONANT INVERTER TOPOLOGY

2.1 SCHEMATIC AND DEFINITION OF CIRCUIT LOOPS

The schematic of the class-E resonant inverter topology is shown in Figure 1. Figures 2,

3, and 4 define names for the three main circuit loops of the topology used for analysis.
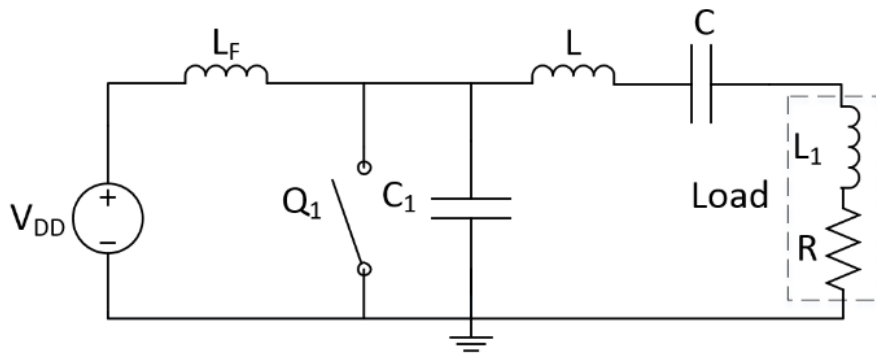
Figure 1 Schematic of the class-E resonant inverter
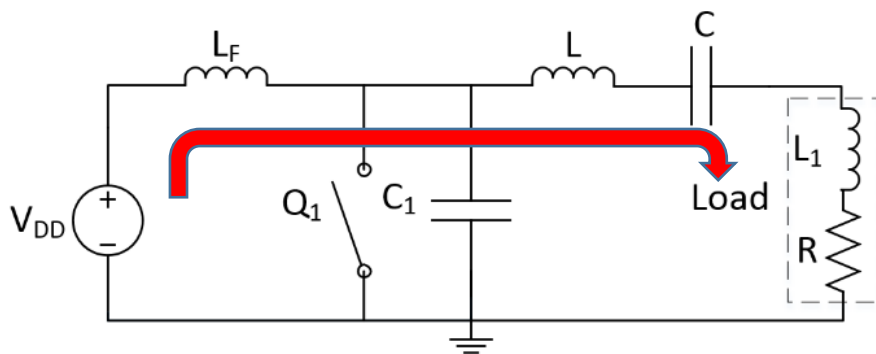
Figure 2 Circuit loop A defined
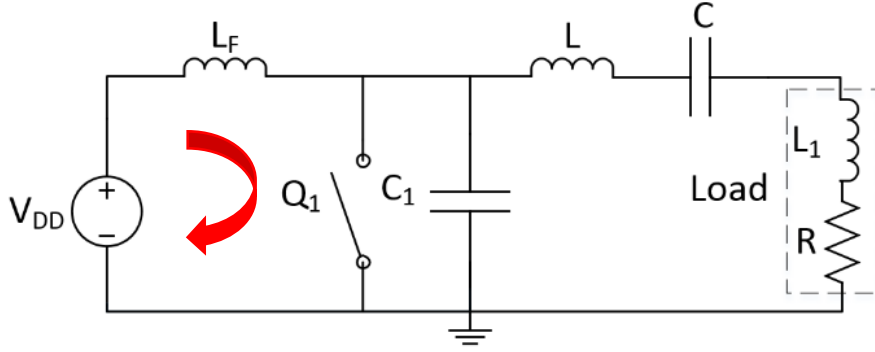
Figure 3 Circuit loop B defined
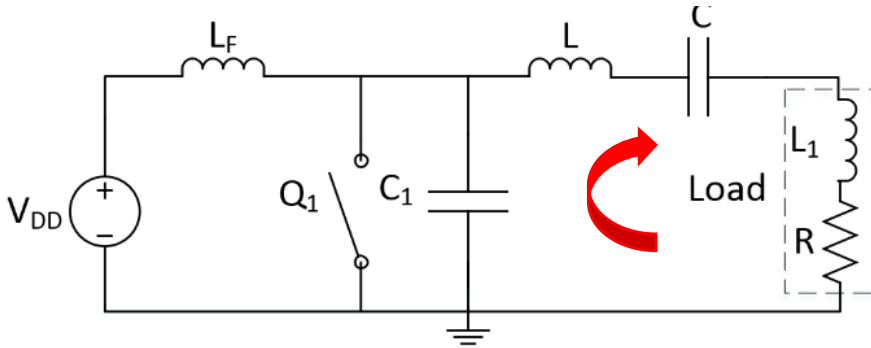
Figure 4 Circuit loop C defined

2.2 RESONANT FREQUENCIES

Four different resonant frequencies exist within the circuit and the way they are designed has a significant impact on the circuit performance. During the on and off states of Q_1 a resonant frequency is generated from circuit elements L_F, L, C and L_1 within circuit loop A as defined in Equation (2.2.1).

$$f_{r,A} = \frac{1}{2\pi\sqrt{(L_F + L + L_1)C_1}}$$

(2.2.1)

During only the on-state of Q_1 a resonant frequency is generated from circuit elements L and C within circuit loop C as defined in Equation (2.2.2).

$$f_{r,C_{\text{on}}} = \frac{1}{2\pi\sqrt{LC}} \qquad (2.2.2)$$

During only the off-state of Q_1 circuit elements L_F and C_1 within circuit loop B generate a resonant frequency as defined in Equation (2.2.3) and circuit elements C_1, L, C and L_1 within circuit loop C generate a resonant frequency as defined in Equation (2.2.4).

$$f_{r,\text{B}} = \frac{1}{2\pi\sqrt{L_F C_1}} \qquad (2.2.3)$$

$$f_{r,C_{\text{off}}} = \frac{1}{2\pi}\sqrt{\frac{1 + \frac{C_1}{C}}{(L + L_1)C_1}} \qquad (2.2.4)$$

2.3 LOAD DEFINITION

The load is defined as, Z, in Equation (2.3.1). Load resistance, R, and inductance, L_1, may be calculated according to Equations (2.3.2) and (2.3.4), respectively. An optimum load, Z_{OPT}, exists where ZVS and ZDS requirements are satisfied.

$$Z = R + j\omega L_1 \qquad (2.3.1)$$

$$R = Z \times PF \qquad (2.3.2)$$

$$X_L = \sqrt{\left(\frac{R}{PF}\right)^2 - R^2} \qquad (2.3.3)$$

$$L_1 = \frac{2\pi f}{X_L} \tag{2.3.4}$$

Three regions of load operation are defined: 1.) $Z < Z_{OPT}$ 2.) $Z = Z_{OPT}$ and 3.) $Z > Z_{OPT}$. In Region 1, reduction of impedance causes decreased damping of V_S beneath zero volts before Q_1 turns on. In practice when a MOSFET is utilized, the intrinsic reverse body diode of the switching device is activated effectively reducing the switch voltage to zero instead of a negative value. While ZVS may seem in effect in Region 1 due to reverse body diode voltage, it is impossible to achieve ZDS at turn-on transient, resulting in increased power switching losses. In Region 2, Z_{OPT} triggers the exact damping of V_S required at $f_{r,C_{off}}$ to achieve ZVS and ZDS simultaneously. In Region 3, an increased impedance causes over-damping of V_S and thus, during the turn-on process of Q_1, neither ZVS nor ZDS can be realized. A visual concept of the three defined impedance regions is shown in Figure 5 below.
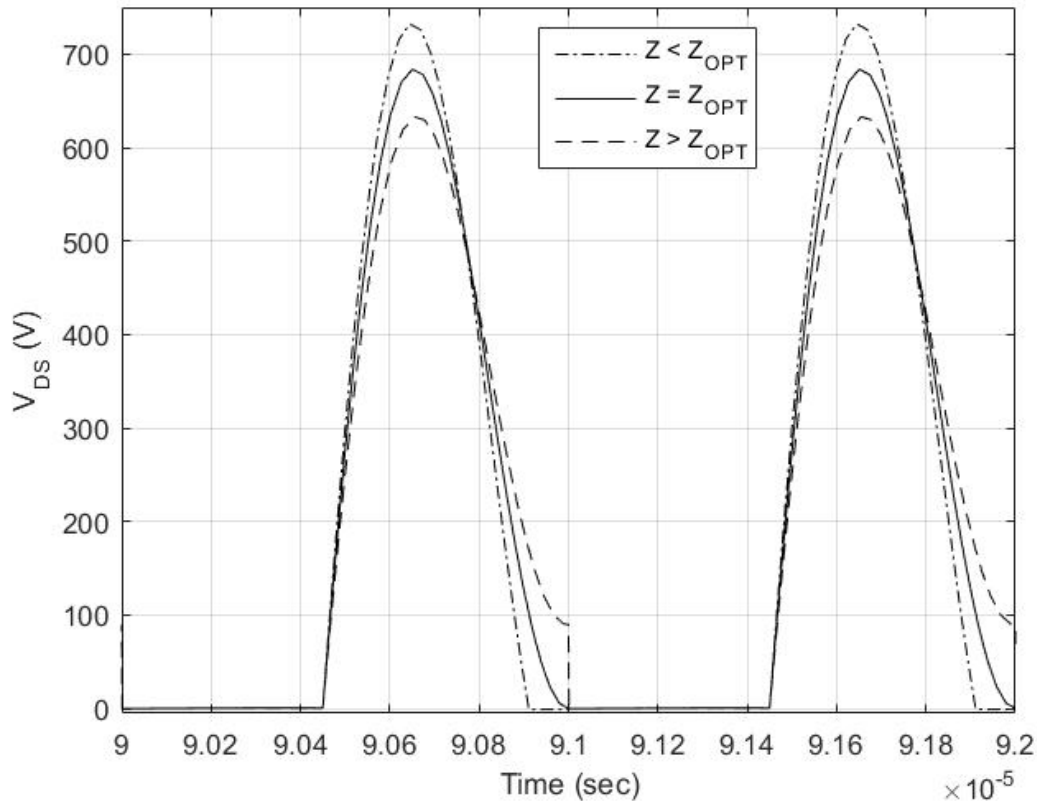
Figure 5 Three regions of load operation for the class-E topology using MOSFET as switching device

2.4 CHOKE INDUCTOR, L_F

The primary purpose of the choke inductor, L_F, is to limit oscillation of I_{DD} to protect the frontier DC voltage source and improve power quality. Figure 6 shows the effect of L_F on I_{DD} when all other circuit elements than L_F remain constant. Often in practice these positive and negative amplitudes are required to be within five percent of each other. As described in Equation (2.4.1), the increase of switching frequency, f_{SW}, in Q_1 would reduce the inductance of L_F, which is required to achieve the same impedance X_{L_F} to meet the design criteria of five percent current oscillation.

Increased choke inductance causes decreased V_S and P_O capability. Figure 7 shows the effect of L_F on P_O and V_S when all other circuit elements than L_F remain constant. L_F should therefore be designed to limit I_{DD} oscillation while limiting the maximum amplitude of V_S to capability of the selected switching device and allowing the required power output.

$$X_{L_F} = 2\pi f_{SW} L_F \qquad (2.4.1)$$
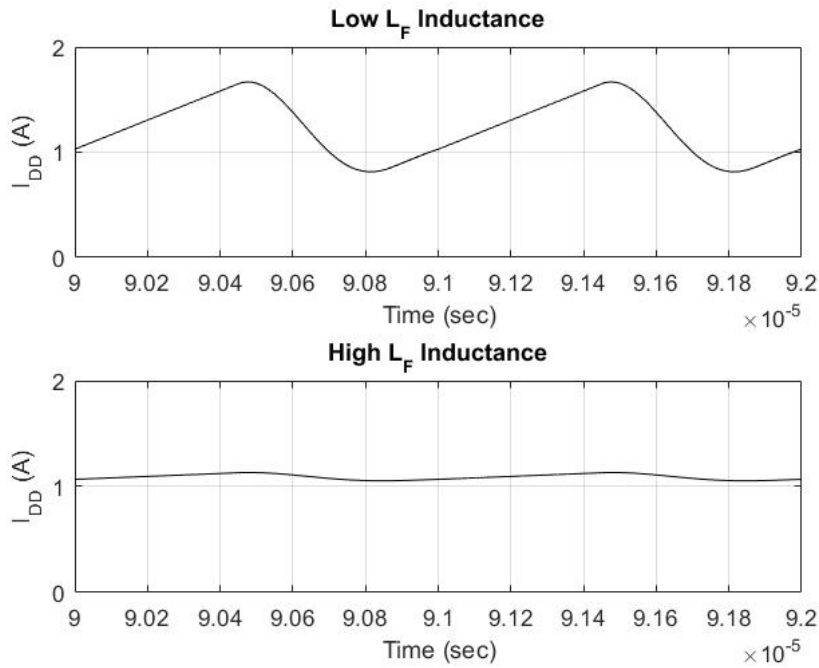
Figure 6 I_{DD} comparison of design with low L_F inductance and high L_F inductance
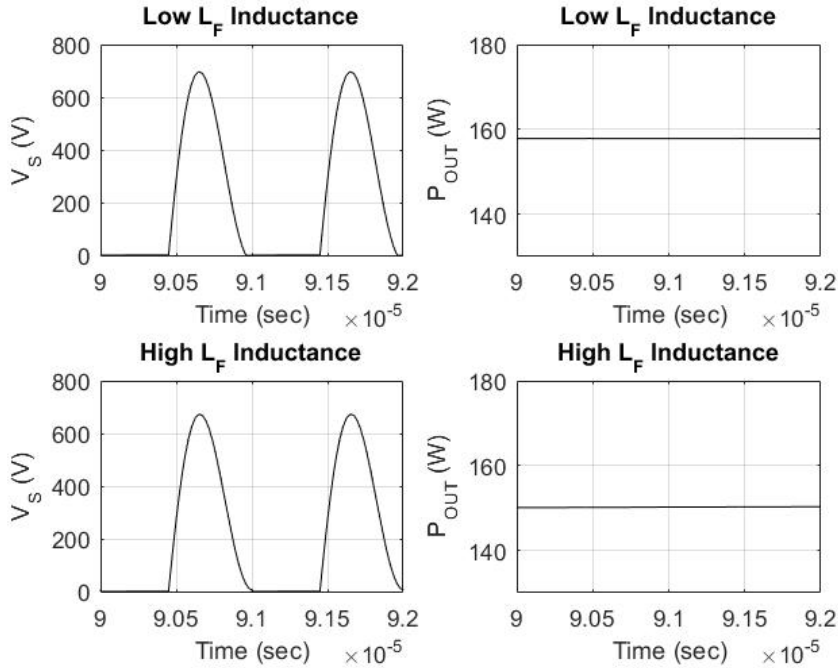
Figure 7 P_O and V_S comparison of design with low L_F inductance and high L_F inductance

2.5 LC RESONANT TANK CIRCUIT

The purpose of inductor, L, and capacitor, C, is to establish $f_{r,Con}$ and $f_{r,Coff}$ near the switching frequency, f_{SW}. This under-damped circuit establishes I_O and portrays a sinusoidal switch voltage which allows C_1 to controllably charge and discharge during the off state of Q_1 so that ZVS and ZDS may be achieved. The description of how under-damped the oscillation may be described by the load quality factor, or Q_L, according to Equation (2.5.1). A higher Q_L allows a lower rate of energy loss but is less effective for a wide range of frequencies. This allows oscillations to occur longer with less dampening. However, a higher Q_L causes more stress on circuit components.

$$Q_L = \frac{2\pi f_{SW}(L + L_1)}{R} \qquad (2.5.1)$$

2.6 SHUNT CAPACITANCE, C_1

The shunt capacitance, C_1, enables designed control of V_S to realize ZVS and ZDS during the switch transition from off-state to on-state. It also establishes $f_{r,Coff}$ during the off-state of the switch such that f_{SW} is between $f_{r,Con}$ and $f_{r,Coff}$. The difference between $f_{r,Con}$ and $f_{r,Coff}$ contributes to impurity of the I_O. To reduce this impurity, C_1 should be minimized so that $f_{r,Con}$ and $f_{r,Coff}$ can be as closely related as possible to f_{SW}.

2.7 SWITCH DUTY CYCLE, D

The switch duty cycle contributes to the class-E circuit's output power, efficiency, and voltage stress on Q_1. Larger duty ratios offer the highest efficiency but with reduced circuit power output capability and increased voltage stress on Q_1. Smaller duty ratios offer less circuit efficiency but with less voltage stress on Q_1. Duty cycles within the 0.35 to 0.65 range offer the optimum operating point considering maximum power output capability, voltage stress on Q_1, efficiency. The highest power output capability is when $D = 0.5$ [27], [29], [30]. Circuit components may be tuned to allow ZVS and ZDS operation based on the duty cycle chosen.

CHAPTER 3

DESIGN OF A CLASS-E RESONANT INVERTER

3.1 BASIC REQUIREMENTS

A voltage supply, V_{DD}, of 208 V was chosen based on its acceptance in modern data center and electric vehicle charging applications. The switching frequency was chosen as 1 MHz in aim to achieve higher power density and provide a more efficient transmitter frequency than modern WPT systems. Target output power was defined at 150 W with the goal to realize an experimental test bed and provide a reference point for future work to achieve higher power output using the 208 V supply voltage.

3.2 BRUTE FORCE MATHEMATICAL DESIGN PROCEDURES

The class-E circuit topology can be described by a group of the second order differential equations shown in Equations (3.2.1), (3.2.2), (3.2.3), and (3.2.4). These equations are derived using KCL and KVL for the nodes and loops within the circuit. Solving these equations to determine component values requires brute force analytical techniques using the class-E optimum conditions as no such explicit solution has yet been known to be discovered.

During the on-state of Q_1,

$$V_{DD} - I_{DD_{on}}(t)R_{DS(on)} + I_O R_{DS(on)} \cos(\omega t + \phi) = L_F \frac{d^2 I_{DD_{on}}(t)}{dt^2} \tag{3.2.1}$$

$$C_1 \frac{d^2 V_{S_{on}}(t)}{dt^2} + \frac{1}{R_{DS(on)}} \frac{dV_{S_{on}}(t)}{dt} - \frac{V_{DD} - V_{S_{on}}(t)}{L_F} - \omega I_O \cos(\omega t + \phi) = 0 \tag{3.2.2}$$

During the off-state of Q_1:

$$L_F C_1 \frac{d^2 I_{DD_{off}}(t)}{dt^2} + I_{DD_{off}}(t) = I_O \cos(\omega t + \phi) \tag{3.2.3}$$

$$L_F C_1 \frac{d^2 V_{S_{off}}(t)}{dt^2} + V_{S_{off}}(t) - V_{DD} - \omega L_F I_O \cos(\omega t + \phi) = 0 \qquad (3.2.4)$$

In this work, no solution was found using brute force techniques based on Equations (3.2.1),

(3.2.2), (3.2.3), and (3.2.4) with class-E conditions. Other researchers have had similar results using

brute force techniques [26], [27]. Ideally, no assumptions are made in the design for increased

accuracy and performance. Because the scope of this work is to examine load sensitivity, the

design will be established using assumptions and simulation validation.

3.3 ASSUMPTIONS USED TO SIMPLIFY DESIGN PROCEDURE

The Q_1 duty cycle was chosen as 0.45 to optimize the performance of the circuit and limit

the maximum amplitude V_S to device capabilities [30]. The load resistance was chosen as 100 Ω

for PF 1.0 load. The design requires the ripple of the input current to be less than five percent of

its RMS value. The selection of L_F according to Equation (3.3.1) presented within [16] was causing

more than desirable current ripple. To simplify the design, choke inductor, L_F, was selected as 1.5

mH, which is approximately two times the inductance suggested in [16].

$$L_F = \frac{7R}{f} \qquad (3.3.1)$$

In summary, the component values are as described in the table below, which were used in the

design procedure to be presented.

Table 1 Summary of design values defined and assumed

V_{DD}	208 V
F_{SW}	1 MHz
D	0.45
P_O	150 W
L_F	1.5 mH

Q_L	6
R	100 Ω

3.4 DESIGN PROCEDURE

The key assumptions used with this approach were the following [23], [29]:

1) L_F is large enough to neglect its current ripple.

2) Internal resistance of L_F is zero and the DC voltage drop across L_F is zero.

3) Q_L of the resonant circuit is high enough so that the output current can be considered as a pure sinusoidal wave.

4) Load resistance includes parasitic resistances of the resonant circuit such that the resonant circuit is considered as a pure reactance.

5) Internal resistance of the switching device is neglected and equal to zero.

6) Turn-on and turn-off times of switching device are neglected and as a result Q_1 turns on and off instantly.

7) ZVS and ZDS conditions are satisfied.

8) C_1 is constant and not influenced by other parameters.

Equations (3.4.1) through (3.4.11) were used to select component values shown in Table 2. While the load resistance was predefined already in Table 1, Equation (3.4.2) was still used when selecting dependent component values. Figure 8 shows the mathematical defined V_S using Equation (3.4.11) and component values shown in Table 2. These results validate ZVS and ZDS conditions were satisfied according to mathematical analysis.

$$\phi = \tan^{-1}\left[\frac{\cos(2\pi D) - 1}{2\pi(1 - D) + \sin(2\pi D)}\right] + n\pi \qquad (3.4.1)$$

$$R = 2 \frac{V_{DD}^2 \sin^2(\pi D) \sin^2(\pi D + \phi)}{\pi^2 (1 - D)^2 P_O} \tag{3.4.2}$$

$$C_1 = \frac{P_O (1 - D) \cos(\pi D + \phi) [\pi(1 - D) \cos(\pi D) + \sin(\pi D)]}{\omega V_{DD}^2 \sin(\pi D + \phi) \sin(\pi D)} \tag{3.4.3}$$

$$L = \frac{Q_L R}{\omega} \tag{3.4.4}$$

$$a_1 = \cos(2\pi D) - \pi(1 - D) \sin(2\pi D) \tag{3.4.5}$$

$$a_2 = (1 - D)\pi \cos(\pi D) + \sin(\pi D) \tag{3.4.6}$$

$$L_b = \frac{R}{\omega} \frac{2(1 - D)^2 \pi^2 - 1 + 2 \cos \phi \cos(2\pi D + \phi) - \cos(2\pi D + 2\phi) a_1}{4 \sin(\pi D) \cos(\pi D + \phi) \sin(\pi D + \phi) a_2} \tag{3.4.7}$$

$$C = \frac{1}{\omega^2 (L - L_b)} \tag{3.4.8}$$

$$b_1 = \frac{V_{DD} \tan(\pi D + \phi) \sin(\pi D)}{(1 - D)[\pi(1 - D) \cos(\pi D) + \sin(\pi D)]} \tag{3.4.9}$$

$$b_2 = \frac{2\pi(1 - D)[\cos(\omega t + \phi) - \cos(2\pi D + \phi)]}{\cos(2\pi D + \phi) - \cos \phi} \tag{3.4.10}$$

$$V_s = b_1(\omega t - 2\pi D + b_2) \tag{3.4.11}$$

Table 2 Summary of components calculated using information provided in Table 1 and Equations (3.4.2), (3.4.3), (3.4.4) and (3.4.8)

R	122.13 Ω
C_1	284.94 pF
L	116.62 μH
C	282.31 pF
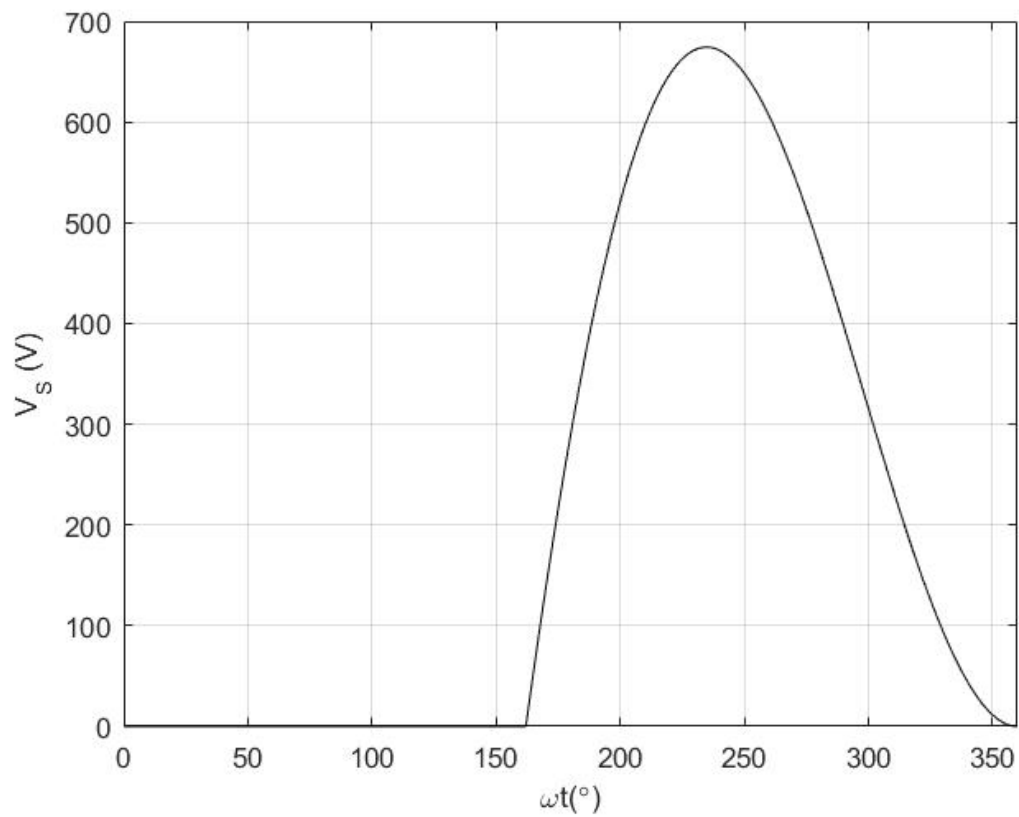
Figure 8 Validation using Equation (3.4.11) that components selected using mathematical analysis satisfy ZVS and ZDS conditions

3.5 SIMULATION RESULTS OF DESIGN BASED ON KAZIMIERCZUK'S DESIGN EQUATIONS

Several key mathematical assumptions were required to determine the component values listed in Table 2. This section provides simulation analysis to validate and further improve the design of these components using fewer assumptions. Assumptions are still required for this process and include:

1) L_F is large enough to neglect its current ripple.

2) Internal resistance of L_F is zero and the DC voltage drop across L_F is zero.

3) Internal resistance of Q_1 is considered and a non-zero value.

4) Turn-on and turn-off times of switching device are neglected and thus Q_1 turns on and off instantly.

5) C_1 is constant and not influenced by other parameters.

For this analysis the metal oxide semiconductor field-effect transistor (MOSFET) was selected and modeled as the switching device because of its higher power capability at higher switching frequencies than insulated bipolar transistors (IGBTs). The specific MOSFET, described in Table 3, utilizes SiC technology, which offers higher efficiency and temperature withstand than Si technology.

Table 3 Semiconductor devices selected as Q_1 for analysis

Technology	Manufacturer	Part Number	$R_{DS(on)}$
SiC MOSFET	CREE	C2M0280120D	$280m\Omega$

Figure 9 shows the $V_{DS}(t)$ plot for the design using parameters from Tables 1 and 2 and the SiC MOSFET manufactured by CREE with part number C2M0280120D. The simulation showed P_O approximately equal to 162 W and under not ideal switching conditions.
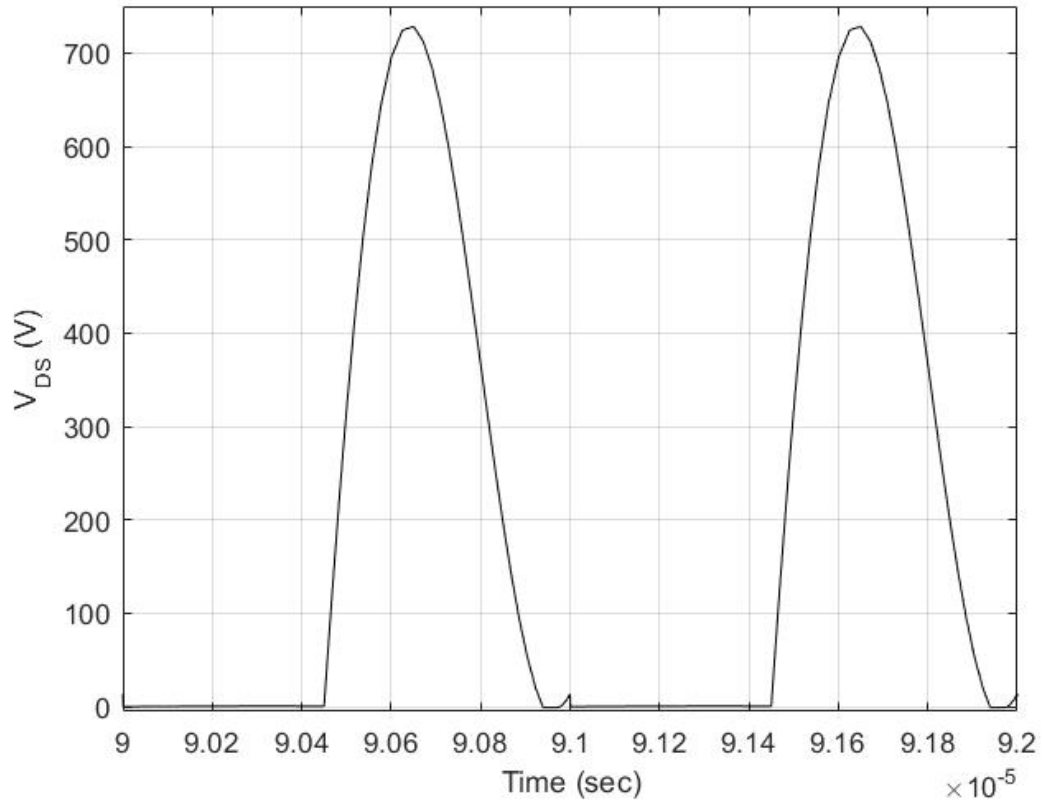
Figure 9 Simulation of design using components values in Tables 1 and 2 and $R_{DS(on)}$=280 mΩ

3.6 TUNING OF DESIGN BASED ON KAZIMIERCZUK'S EQUATIONS

Components determined and listed in Table 2 were tuned to achieve optimum conditions using simulation. While the target was to ultimately maintain $R = 100 \ \Omega$ and $Q_L = 6$, these parameters were adjusted to achieve damping and output power as required for ZVS and ZDS. Table 4 shows the component values selected from tuning based on simulation analysis. The resultant ZVS and ZDS plots from this improved design are shown in Figure 10. The following basic guidelines were followed until the optimum design goals were reasonably achieved:

- When the Q_1 voltage is below zero volts at the moment of Q_1 turn-on, increase C_1 or increase R.

- When the Q_1 voltage is above zero volts at the moment of Q_1 turn-on, decrease C_1 or decrease R.

- When more P_O is required increase Q_L or make $f_{r,Con}$ and $f_{r,Coff}$ closer to f_{SW}.

- When less P_O is required decrease Q_L or make $f_{r,Con}$ and $f_{r,Coff}$ farther from f_{SW}.

Table 4 Design values after tuning based on simulation analysis

R	105.78 Ω
C_1	360 pF
L	96 μH
C	360 pF
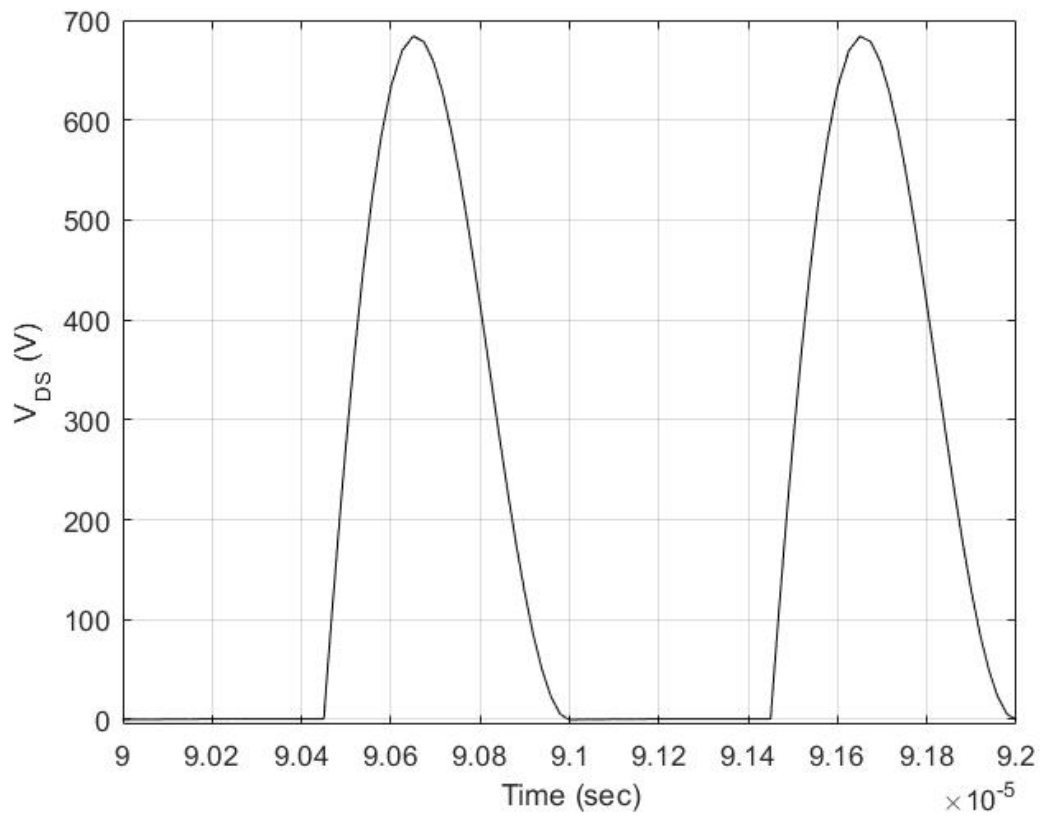
Figure 10 Using components designed listed in Table 4, $P_O = 154.56$ W

CHAPTER 4

STEADY STATE LOAD ANALYSIS USING SIMULATION

4.1 ASSUMPTIONS

Key assumptions used for the simulation analysis were the following:

1) L_F is finite and input current ripple exists.

2) Internal resistance of Q_1 is considered and a non-zero value.

3) No parasitic resistances exist throughout the circuit.

4) Turn-on and turn-off times of switching device are neglected and thus Q_1 turns on and off

   instantly.

5) C_1 is constant and not influenced by other parameters.

6) Output power is calculated by using the instantaneous load voltage and load current

   multiplied together and averaged over one cycle.

4.2 METHODOLOGY

Each simulation was performed using final design values shown in Table 5. The $R_{DS(on)}$,

L_1, and R component values varied for each simulation. Two different Si and SiC MOSFET

switching device models shown in Table 6 were used to determine the effect of $R_{DS(on)}$ on the load

and ZVS and ZDS performance. The load impedance required for ZVS and ZDS operation for

each load and device combination were determined by modifying the load parameters, L_1 and R,

within the simulation until the optimum performance was found. The P_O, V_O, I_O, and efficiency

values for each load and device combination were calculated. The load consisted of impedance

values in the range of 20 Ω to 200 Ω, in increments of 10 Ω. Load parameters, R and L_1, required

to achieve each impedance value in range of 20 Ω and 200 Ω were determined by using Equations

(2.3.2) and (2.3.4).

Table 5 Component values used in each simulation

V_{DD}	208 V
f_{SW}	1 MHz
D	0.45
L_F	1.5 mH
C_1	360 pF
L	96 μH
C	360 pF

Table 6 Semiconductor devices selected as Q_1 for analysis

Technology	Manufacturer	Part Number	$R_{DS(on)}$
Si MOSFET	Microsemi Inc.	APT7M120B	1.5 Ω
SiC MOSFET	CREE Inc.	C2M0280120D	280 mΩ

4.3 RESULTS

Table 7 lists the load impedances required for ZVS and ZDS for 1.0 and 0.8 power factor loads for both of the Si and SiC MOSFETs. The ZVS and ZDS performance of the SiC MOSFET for 1.0 and 0.8 power factor loads is shown in Figure 11. Figures 12 and 13 demonstrate the output active power, conversion efficiency, load voltage and load current for 1.0 and 0.8 power factor loads, respectively.

Table 7 Z_{OPT} for various switch types and load power factors determined by simulation

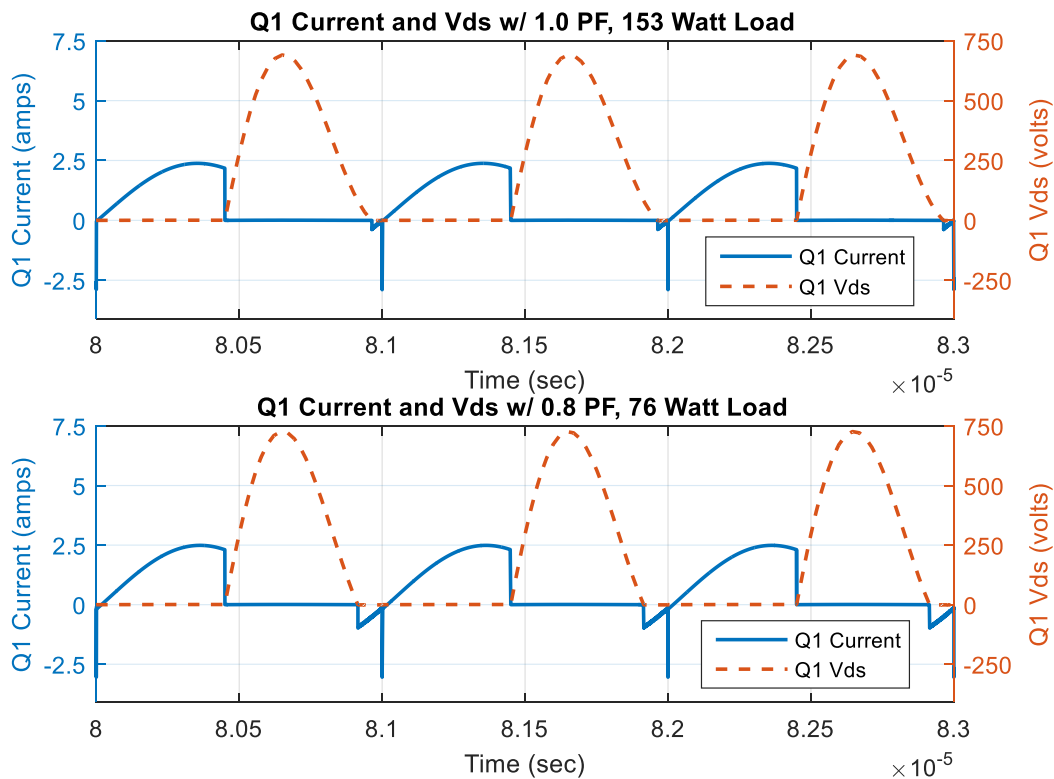| Switch Type	Power Factor	Z_{OPT} (Ω)
Si	1.0	105.3
SiC	1.0	105.9
Si	0.8	119.1
SiC	0.8	119.5

Figure 11 ZVS and ZDS plots for 1.0 and 0.8 power factors loads respective to top and bottom charts
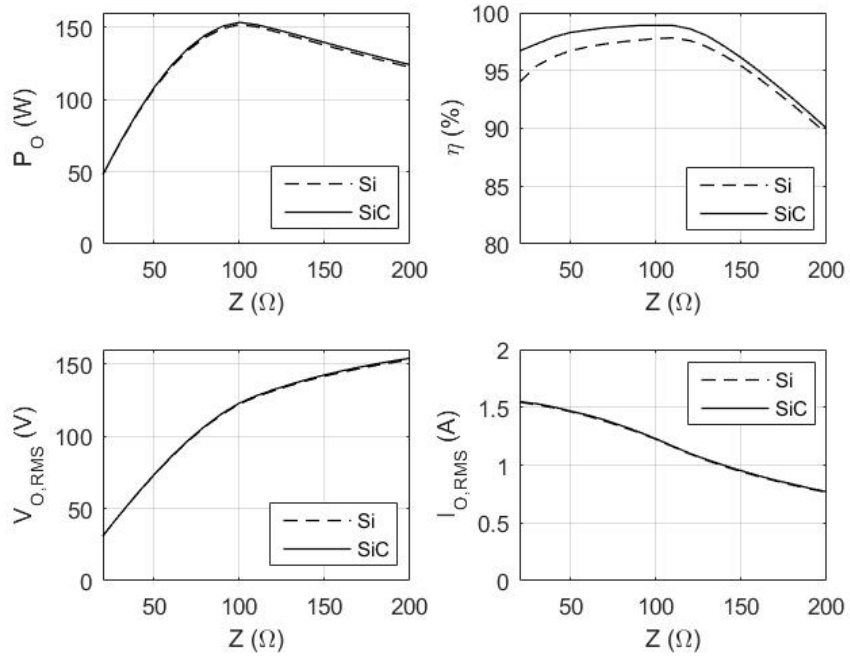
Figure 12 Simulation results for 1.0 power factor load
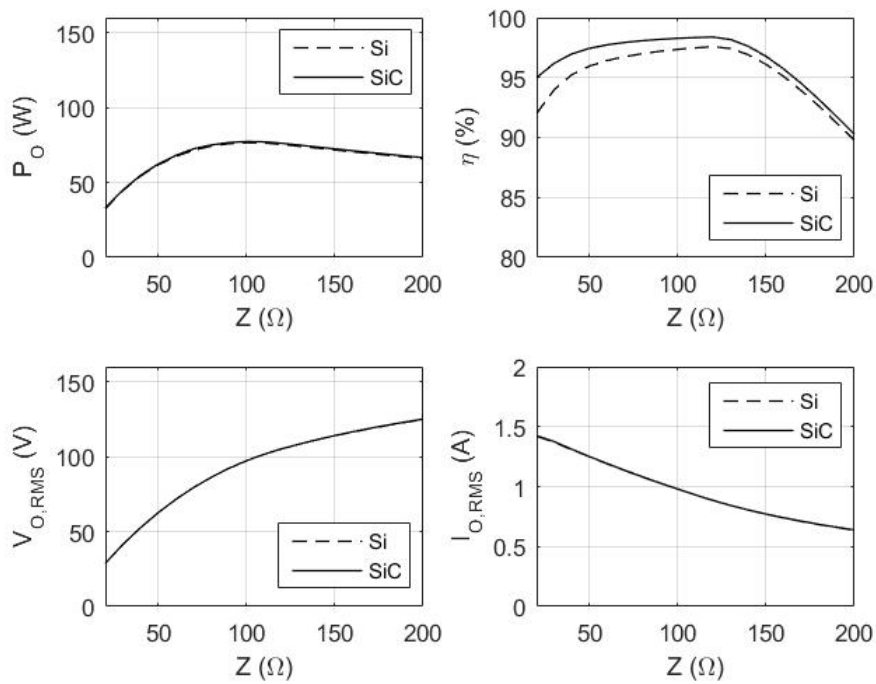
Figure 13 Simulation results for 0.8 power factor load

4.4 ANALYSIS

Figure 11 shows the resonant frequency increases for a 0.8 power factor load compared to a 1.0 power factor load as expected based on Equations (2.2.2) and (2.2.4) for $f_{r,Con}$ and $f_{r,Coff}$. ZVS and ZDS conditions for the 0.8 power factor load was achieved by increasing the impedance to increase dampening of the load waveforms (Table 7).

Figures 12 and 13 show both the 1.0 and 0.8 power factor loads have the highest efficiency at and near Z_{OPT}. However, maximum output capability shown in these figures are not exactly at Z_{OPT}. For 1.0 and 0.8 power factor loads the maximum output power is at approximately 100 Ω impedance. Simulations with load impedances equal to or less than 20 Ω did not achieve steady state performance due to too little dampening and were excluded from the analysis.

Figure 12 shows characteristics of its associated circuits being more underdamped than those shown in Figure 13. This is as expected because the added inductance, L_1, for the power factor 0.8 loads increase the resonant frequency to be further from f_{SW} causing less resonance. The result is almost twice the peak power for the power factor 1.0 load compared to the power factor 0.8 load, but with a higher rate of change of power output capability during variation from Z_{OPT}.

Figure 12 shows the largest difference in conversion efficiency between the Si and SiC models is about 1.14 percent at 100 Ω while Figure 13 shows the largest difference in conversion efficiency between Si and SiC models is about 0.93 percent at 100 Ω. These results show the influence of $R_{DS(on)}$ on conversion efficiency is limited and may reasonably be assumed negligible for all considerations except circuit efficiency in order to simplify mathematical analysis.

In the range of 80 Ω to 140 Ω the power factor 1.0 load remains within five percent of the rated output power and with efficiency greater than 97.1 percent. Above 140 Ω the efficiency and output power decrease at a high rate. Below 80 Ω the output power decreases at a high rate while the efficiency remains above 96.7 percent. In summary, in specific load impedance regions offer reasonable output power and efficiency performance.

In the range of 72 Ω to 150 Ω the power factor 0.8 load remains within five percent of one-half the rated output power and with efficiency greater than 95 percent. Below 72 Ω the output power decreases at a moderate rate while efficiency remains at or above 95 percent. Above 150 Ω the power output decreases at a slow rate while efficiency decreases at a high rate. In summary, for this design the 0.8 power factor load operates reasonably well in the load region 72 Ω to 150 Ω at one-half the designed output power.

Both of the 1.0 and 0.8 power factor loads lack voltage regulation. Consequently, as the load impedance increases the current decreases while the voltage increases (Figures 12 and 13). For WPT applications commonly the received signal is converted to DC and a DC to DC voltage regulator is utilized for end of use voltage control. Further evaluation of voltage regulation at load side is out of the scope of this work.

CHAPTER 5

STEADY STATE LOAD ANALYSIS USING MATHEMATICS

5.1 ASSUMPTIONS

Key assumptions used for the mathematical analysis were the following [23]:

1) L_F is large enough to neglect its current ripple.

2) Internal resistance of L_F is zero and the DC voltage drop across L_F is zero.

3) Q_L of the LC resonant tank is high enough so that the output current can be considered as a pure sinusoidal waveform.

4) Load resistance includes parasitic resistances of the resonant circuit such that the resonant circuit can be considered as a pure reactance.

5) Internal resistance of the switching device is neglected and equal to zero.

6) Q_1 is an ideal switching device.

7) C_1 is constant and not influenced by other parameters.

5.2 EQUATIONS

Equations from [23] were used for the steady-state load analysis using mathematics.

$$i_O(t) = I_O \sin(\omega t + \emptyset) \tag{5.2.1}$$

$$i_S(t) = I_{DD} - I_O \sin(\omega t + \emptyset) \tag{5.2.2}$$

$$V_S(t) = \frac{1}{\omega C_1}[I_{DD}\omega t + I_O \cos(\omega t + \varphi) - I_O \cos \varphi] \tag{5.2.3}$$

$$\emptyset = -\tan^{-1}\left[\left(\frac{1}{4}\cos 4\pi D_1 - \cos 2\pi D_1 + \pi\omega C_1 R + \frac{3}{4}\right)(2\pi D \sin 2\pi D_1 \right.$$
$$+ \cos 2\pi D_1 - 1)$$
$$+ \left(\sin 2\pi D_1 - \frac{1}{4}\sin 4\pi D_1 + \pi\omega C_1 X - \pi D_1\right)(2\pi D \cos 2\pi D_1$$
$$\left. - \sin 2\pi D_1)\right]$$
$$\Big/\left[\left(-\frac{1}{4}\sin 4\pi D_1 - \pi\omega C_1 X + \pi D_1\right)(2\pi D \sin 2\pi D_1 \right.$$
$$+ \cos 2\pi D_1 - 1)$$
$$\left. + \left(\pi\omega C_1 R + \frac{1}{4} - \frac{1}{4}\cos 4\pi D_1\right)(2\pi D_1 \cos 2\pi D_1 - \sin 2\pi D_1)\right]$$

$$(5.2.4)$$

$$I_{DD} = 2\pi\omega C_1 V_{DD} \Big/ \{2\pi^2 D_1{}^2$$

$$+ [(\sin 2\pi D_1 - 2\pi D_1)\cos\emptyset$$

$$+ (\cos 2\pi D_1 - 1)\sin\emptyset]\,[(-2\pi D_1 \cos 2\pi D_1$$

$$+ \sin 2\pi D_1)\cos\emptyset + (2\pi D \sin 2\pi D_1 + \cos 2\pi D_1 - 1)\sin\emptyset]$$

$$\Big/\left[\left(\frac{1}{2}\cos 4\pi D_1 - \cos 2\pi D_1 + \frac{1}{2}\right)\cos\emptyset^2 \right.$$

$$+ \left(-\frac{1}{2}\sin 4\pi D_1 + \sin 2\pi D_1\right)\sin\emptyset\cos\emptyset$$

$$\left. + \left(\pi\omega C_1 R - \frac{1}{4}\cos 4\pi D_1 + \frac{1}{4}\right)\right]\}$$

$$(5.2.5)$$

$$I_m = I_{DD}[(-2\pi D_1 \cos 2\pi D_1 + \sin 2\pi D_1) \cos \emptyset$$

$$+ (2\pi D \sin 2\pi D_1 + \cos 2\pi D_1 - 1) \sin \emptyset]$$

$$/ \left[\left(\frac{1}{2} \cos 4\pi D_1 - \cos 2\pi D_1 + \frac{1}{2} \right) \cos \emptyset^2 \right.$$

$$+ \left(-\frac{1}{2} \sin 4\pi D_1 + \sin 2\pi D_1 \right) \sin \emptyset \cos \emptyset$$

$$+ \left. \left(\pi \omega C_1 R - \frac{1}{4} \cos 4\pi D_1 + \frac{1}{4} \right) \right]$$

$$(5.2.6)$$

$$P_O = \frac{I_O^2 R}{2} \qquad (5.2.7)$$

5.3 METHODOLOGY

Each mathematical calculation for P_O, I_O, and V_S was performed using component values shown in Table 5 to allow comparison of the mathematical results to the simulation analysis. Similar to the simulation analysis, the L_1 and R component values were calculated according to Equations (2.7.2) and (2.7.4) for these simulations. Between impedance values 20 Ω and 200 Ω and in increments of 10 Ω the mathematical calculation was used to record the P_O, V_O, I_O, and efficiency values for each 1.0 and 0.8 power factor load. Equation (5.2.3) was used to plot V_S for one cycle in aim to find the Z_{OPT} for 1.0 and 0.8 power factor loads using mathematical analysis.

Table 8 Component values used in each mathematical simulation

V_{DD}	208 V
f_{SW}	1 MHz
D	0.45
C_1	360 pF
L	96 µH
C	360 pF

5.4 RESULTS

ZVS and ZDS performance using mathematical analysis was unable to be confirmed by using Equation (5.2.3) for any of the impedance values in the range of 20 Ω to 200 Ω and for both 1.0 and 0.8 power factor loads. Figures 14 and 15 compare the output active power and load current for 1.0 power factor and 0.8 power factor loads, respectively, to the simulation results.
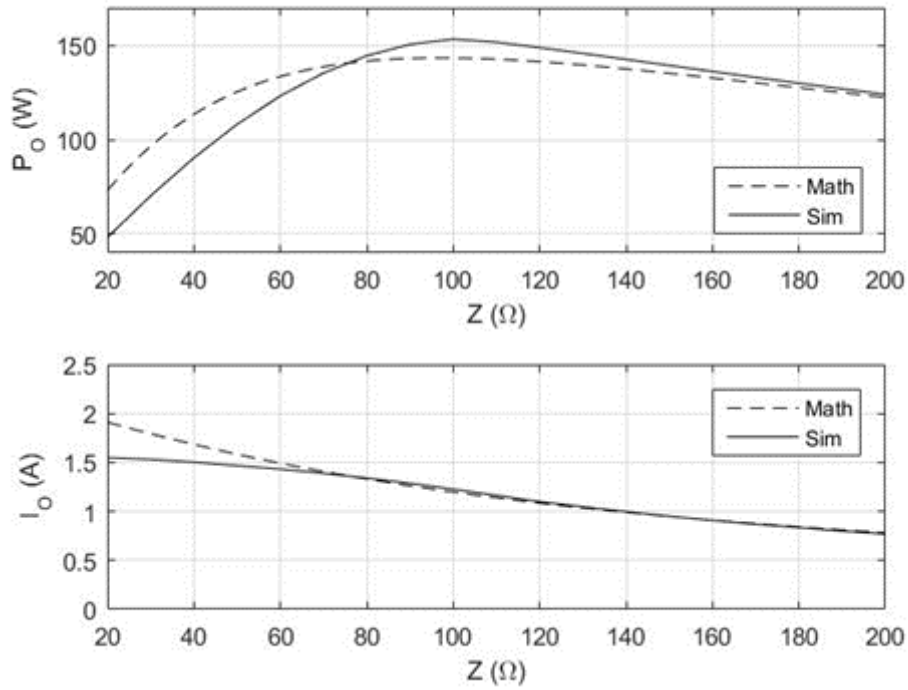
Figure 14 Comparison of math results to simulation results for 1.0 power factor load
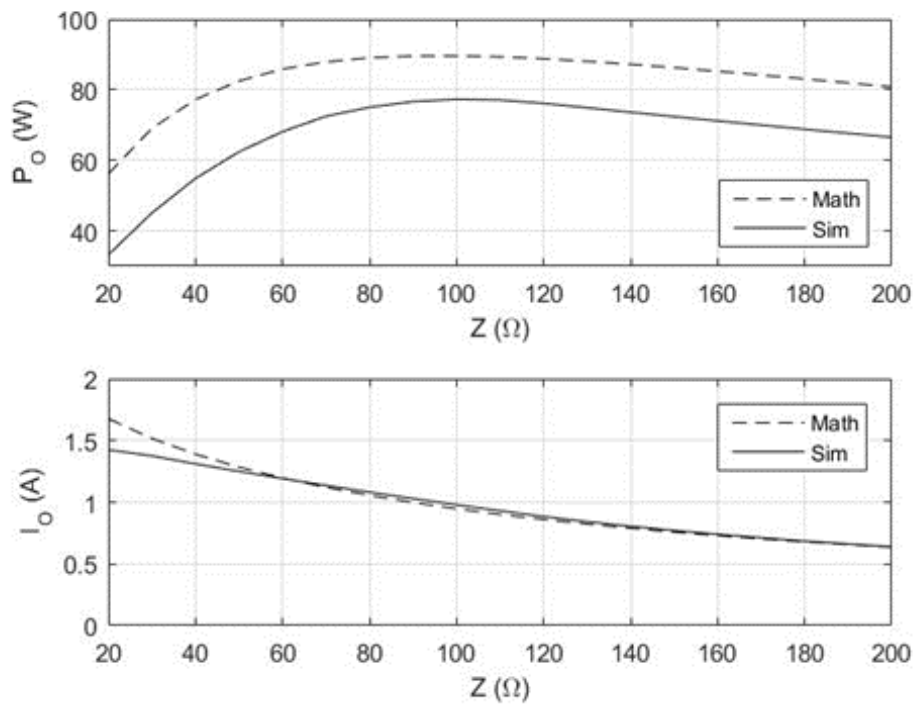

Figure 15 Comparison of math results to simulation results for 0.8 power factor load

5.5 ANALYSIS

Analysis from Section 4.4 show the effect of $R_{DS(on)}$ less than or equal to 1.5 Ω is insignificant on the ECE of the class-E resonant inverter. L_F is designed to maintain ripple current below five percent. These concepts justify simplification of the mathematical analysis significantly by neglecting $R_{DS(on)}$ and assuming no input current ripple.

Figures 14 and 15 show close agreement between the simulated and calculated values of I_O. The difference between the simulated and calculated output power is partly because the mathematical analysis neglected the effects of the anti-parallel diode to Q_1 [23]. This difference is also caused by neglecting the phase difference between I_O and V_O when calculating the output power in the mathematical analysis. Conversely, the simulation analysis did not neglect the phase difference when computing the power output. Therefore, more load reactance results in increased error in output power calculations between the simulation and mathematical analysis. This explains why more error exists in the results of 0.8 power factor load than the 1.0 power factor load. Also, it explains why the calculated output power is approximately 20 W more than the simulated output power for the 0.8 power factor load for impedances 20 Ω to 200 Ω.

Another key reason for the disparity between simulated and calculated output power is the presence of two different resonant frequencies, $f_{r,Con}$ and $f_{r,Coff}$, existing during the on and off states of Q_1. As a result, i_O is not a pure sinusoidal waveform in practice. The RMS value made in both the simulation and the mathematical analysis are an approximation. The power output in simulation analysis considers the impurity of the output current while the mathematical analysis does not. During the off-state, i_O should be in resonance at the frequency of $f_{r,Coff}$, but instead, at f_{SW} due to assumption. Because $f_{r,Coff}$ is greater than f_{SW}, more impedance is needed to dampen V_{DS} in order to achieve ZVS and ZDS.

Ideally, the resonant frequencies, $f_{r,Con}$ and $f_{r,Coff}$, should be close to each other to achieve closely-pure sinusoidal waveform at load. This would improve power quality, reduce noise and increase conversion efficiency.

CHAPTER 6

LOAD ANALYSIS USING EXPERIMENTATION

6.1 METHODOLOGY

Each experiment utilized the same key components on the test bed including control driver, voltage supply, MOSFET, choke inductor, and Schottky diode. A Schottky diode was used in parallel to the MOSFET to allow fast recovery of reverse currents to bypass the MOSFET. Experiments differed from each other by using unique passive components (Table 9). Tuning of the switching frequency and C, R, L, and C_1 component values was performed until ZVS and ZDS conditions for Q_1 were met and recorded as Experiments #1 and #2. Experiments #3 through #10 were performed to analyze varying resistive and inductive load assignments from ideal ZVS and ZDS conditions. Each experiment is numbered on Table 9 and corresponds to a figure showing the experiment's associated $V_{DS}(t)$ and $V_O(t)$ waveforms.

Figure 16 shows a picture of the test bed established to perform experimental testing. It shows the manufactured printed circuit board with associated circuit components mounted to it, signal generator for pulse width modulation, DC power supply for control, DC power supply for power, and an oscilloscope. A custom inductor and resistor bank on bread board is shown to allow easy modification of the load. Appendix A elaborates on the hardware setup used for these experiments.
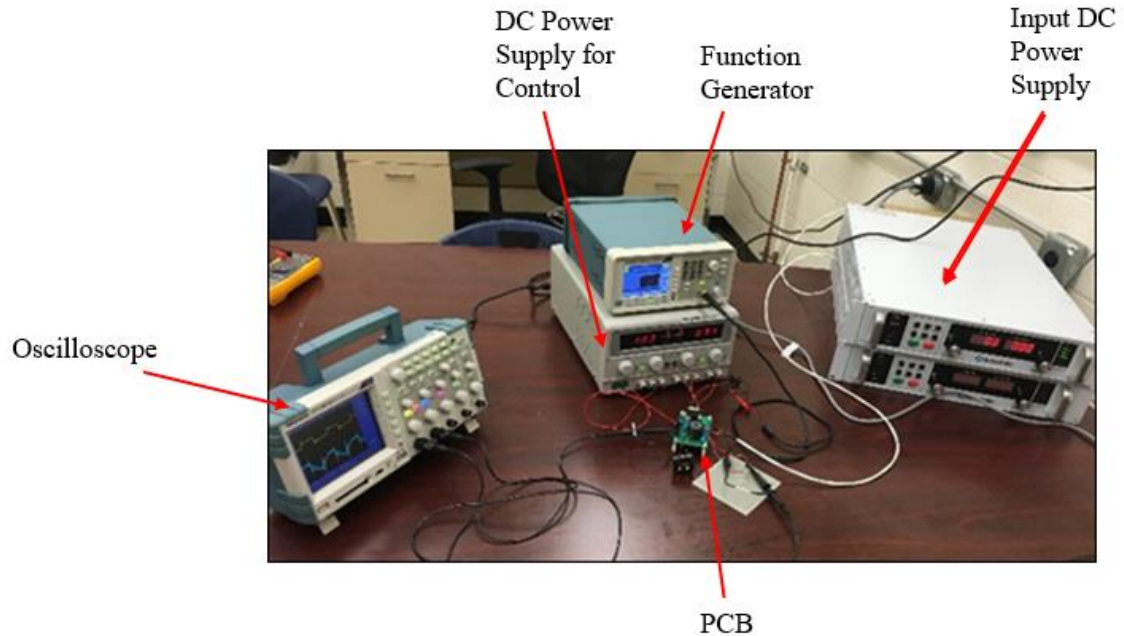
Figure 16 Test-bed of a 150 W class-E resonant inverter prototype

6.2 ASSUMPTIONS

Due to the lack of available voltage probes rated for 1200V, it was assumed that a reduction in supply voltage would not affect the load impedance at which ZVS and ZDS performance was achieved. Simulation was used to validate this assumption. Also, due to limited available hardware in the lab the output power was assumed to be according to Equation (6.2.1).

$$P_O = \frac{V_O{}^2}{2R} \qquad (6.2.1)$$

6.3 RESULTS

Table 9 Component parameters used for each experiment

Experiment #	L_F (mH)	C (nF)	R (Ω)	L (μH)	C_1 (pF)	Duty Cycle	f_{SW} (kHz)	V_{DD} (V)
1	1.5	17.7	50	50	0	0.45	850	40.2
2	1.5	12.1	50	66	0	0.45	850	40.2
3	1.5	23.12	100	50	0	0.45	850	40.2
4	1.5	23.12	150	50	0	0.45	850	40.2
5	1.5	23.12	200	50	0	0.45	850	40.2
6	1.5	23.12	50	50	0	0.45	850	40.2
7	1.5	23.12	400	50	0	0.45	850	40.2
8	1.5	23.12	100	14.74	0	0.45	850	40.2
9	1.5	23.12	300	42.2	0	0.45	850	40.2
10	1.5	23.12	300	42.2	0	0.45	850	40.2

Figure 17 $V_{DS}(t)$ and $V_O(t)$ Waveforms from Experiment #1

Figure 18 V$_{DS}$(t) and V$_O$(t) Waveforms from Experiment #2
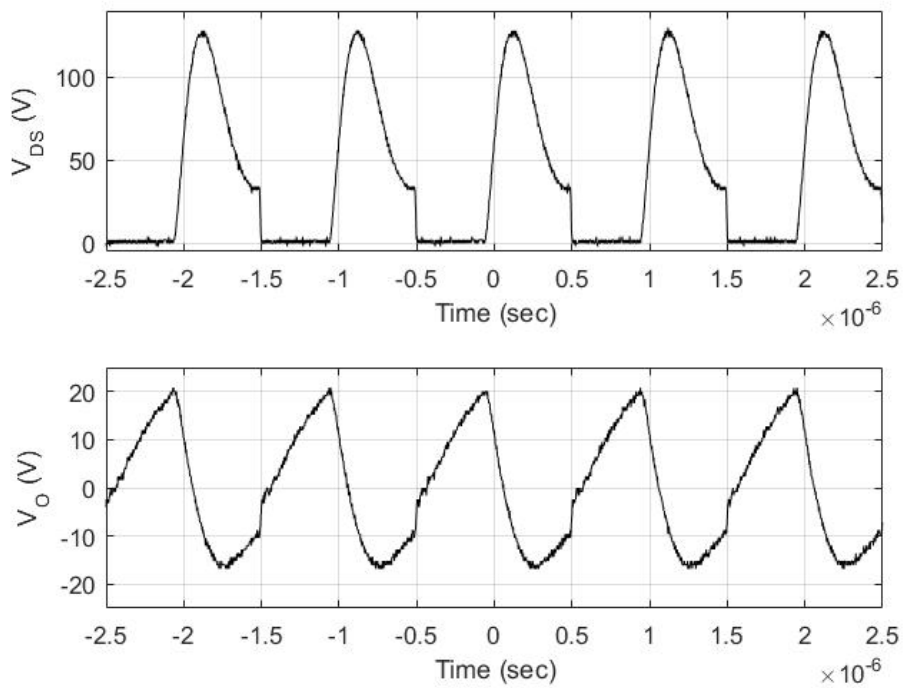
Figure 19 V$_{DS}$(t) and V$_O$(t) waveforms from Experiment #3
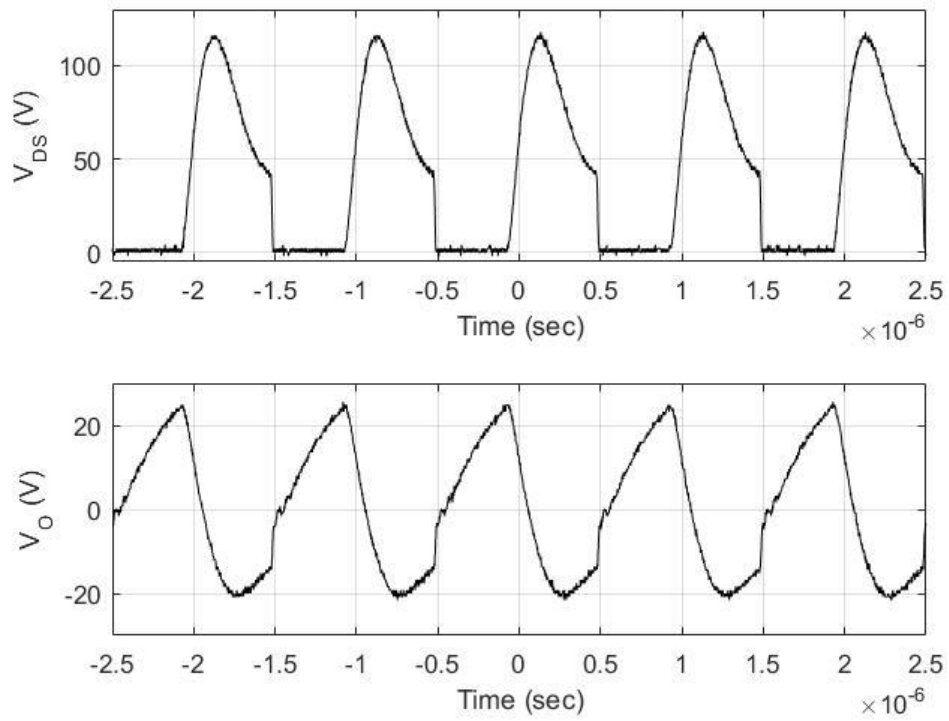
Figure 20 $V_{DS}(t)$ and $V_O(t)$ waveforms from Experiment #4
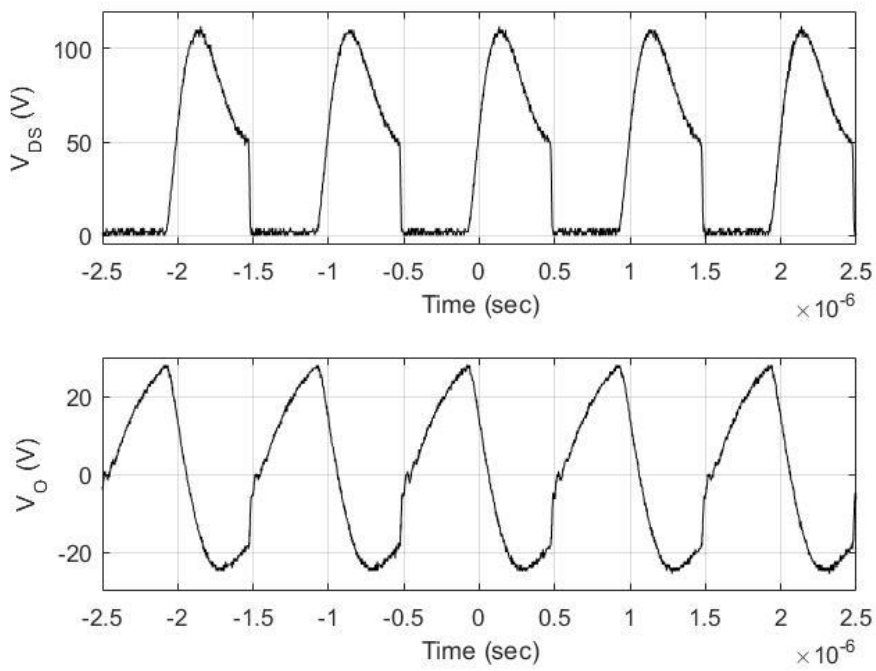
Figure 21 $V_{DS}(t)$ and $V_O(t)$ waveforms from Experiment #5
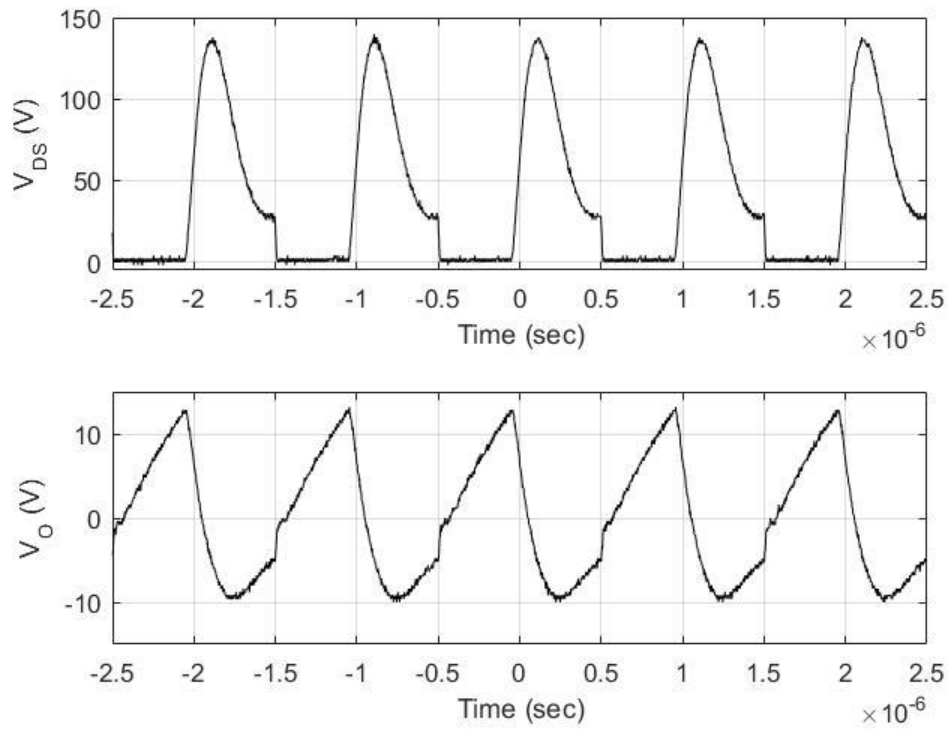
Figure 22 $V_{DS}(t)$ and $V_O(t)$ waveforms from Experiment #6
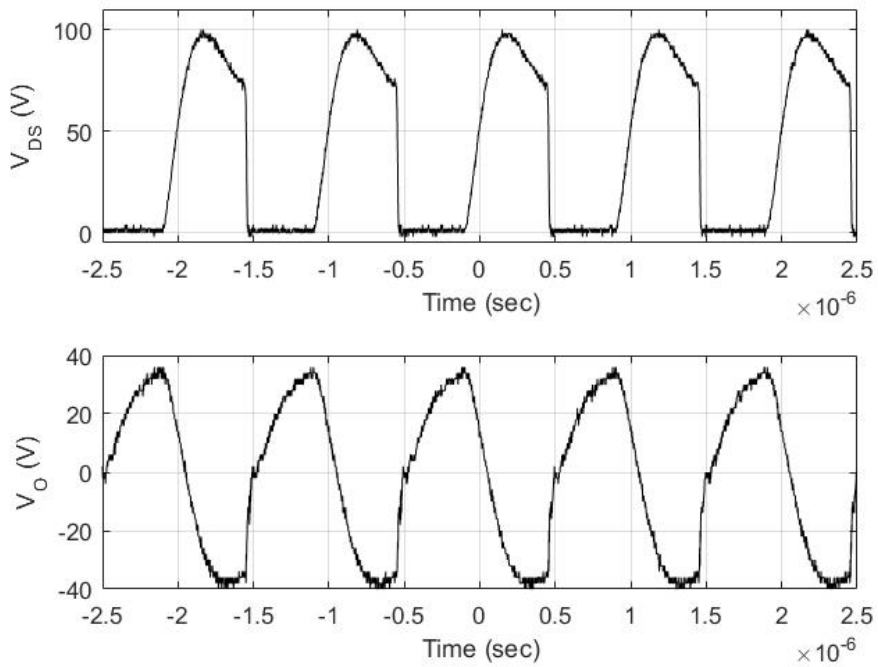
Figure 23 $V_{DS}(t)$ and $V_O(t)$ waveforms from Experiment #7
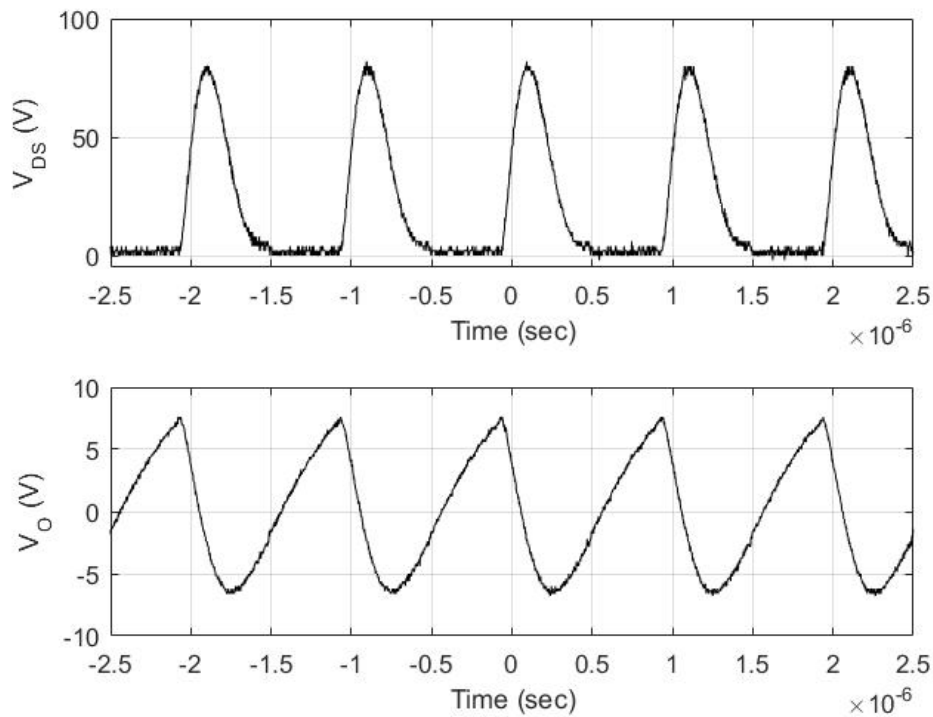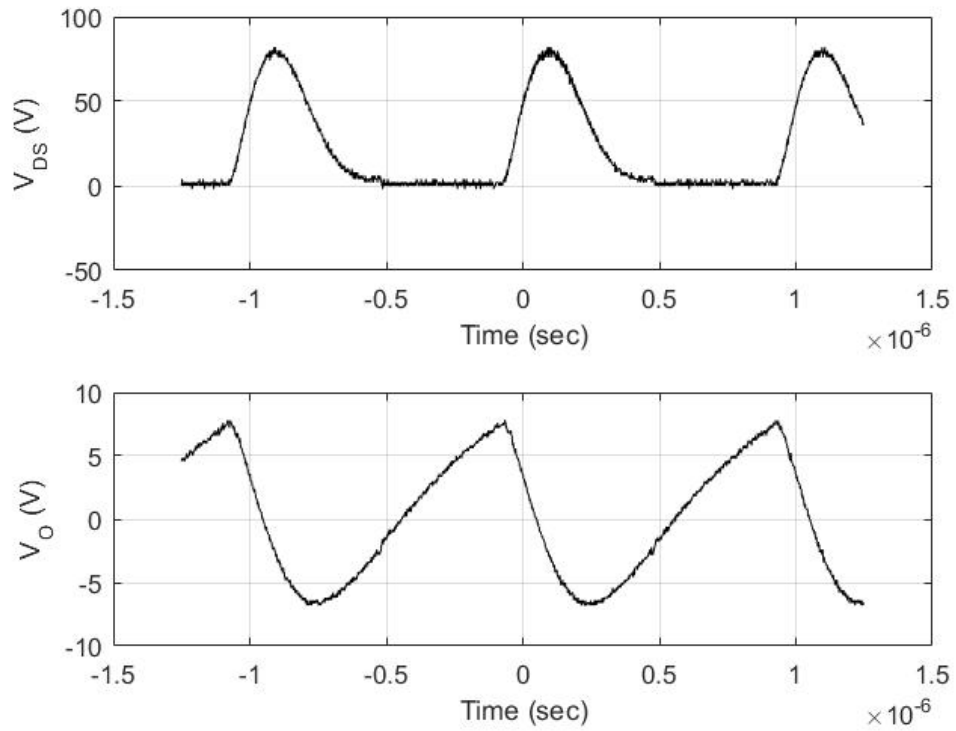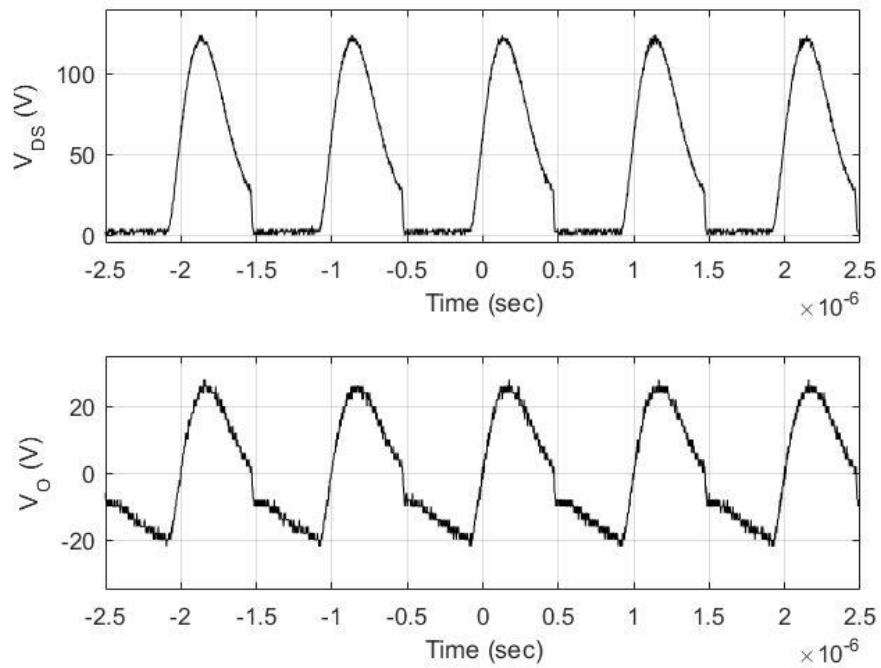
Figure 24 $V_{DS}(t)$ and $V_O(t)$ waveforms from Experiment #8
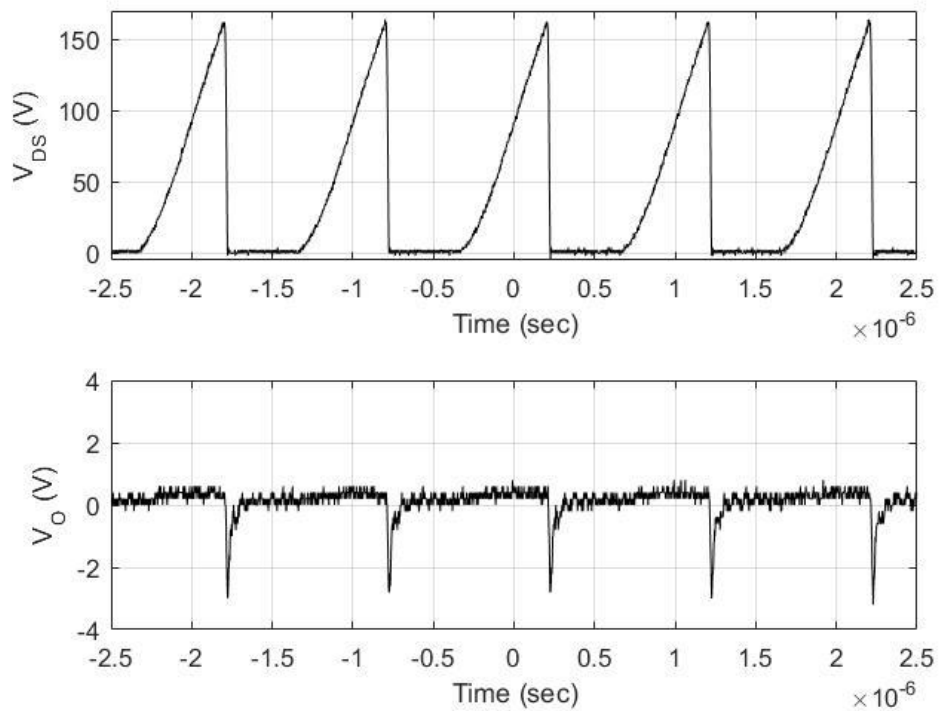
Figure 25 $V_{DS}(t)$ and $V_O(t)$ waveforms from Experiment #9
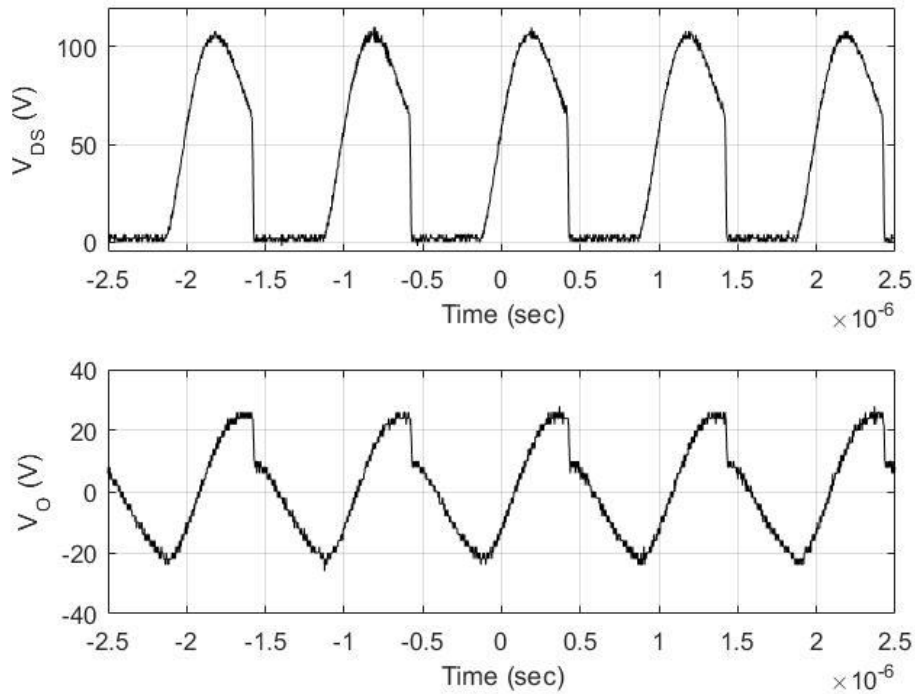
Figure 26 $V_{DS}(t)$ and $V_O(t)$ waveforms from Experiment #10
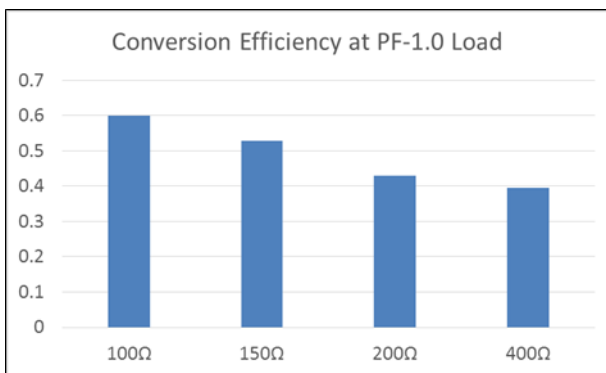
Figure 27 Conversion efficiency of class-E prototype with load resistances 100 Ω, 150 Ω, 200 Ω, and 400 Ω for Experiments #3, #4, #5, and #7, respectively

6.4 ANALYSIS

Achieving ZVS and ZDS operation of Q_1 during experimentation required modifying switching frequency, load impedance, resonant tank parameters, and shunt capacitance from design values. ZVS and ZDS performance of Q_1 was achieved in Experiments #1 and #2 as shown

in Figures 17 and 18, respectively. The optimum design point, Z_{OPT}, where ZVS and ZDS occurred for the experimental test differed from the simulated and calculated results because of the parasitic effects in the circuit dampened the resonance and the nonlinear shunt capacitance formed from the MOSFET and Schottky diode. In order to achieve ZVS and ZDS the switching frequency had to be reduced from 1 MHz to 850 kHz. The resonant frequency, $f_{r,Coff}$, generated by the resonant tank reduced the design from 1.2107 MHz to a calculated value of 161.8 kHz. By reducing f_{SW} and $f_{r,Coff}$ less parasitic influence on the resonant waveforms allowed ZVS and ZDS operation to be achieved. While the calculated resonant frequency is 161.8 kHz, f_{SW} is equal to 850 kHz and it is therefore unlikely that the calculated resonant frequency is accurate on the test bed and in reality much higher than 161.8 kHz.

Experiments #3 through #10 focused on observation of load waveforms varying from this optimum performance. Also, the ECE of load impedances 100 Ω, 150 Ω, 200 Ω, and 400 Ω were analyzed using Equation (6.2.1) to calculate P_O and information from the DC power supply to calculate input power. V_O plots shown in all experiments (see Figures 17 through 26) clearly show two different resonant frequencies formed for on and off cycles of Q_1. As expected, loads with more impedance increased circuit dampening and resulted in a loss of conversion efficiency as described in Figure 27 for experiments utilizing load impedances of 100 Ω, 150 Ω, 200 Ω, and 400 Ω in Figures 19, 20, 21, and 23, respectively. Because of parasitic influence and assumptions used for output power calculation which neglected phase difference between V_O and I_O, the output power results are significantly different from the simulation and mathematical results. However, these experiments show important considerations that should be used in future research and experimentation.

CHAPTER 7

CONCLUSIONS AND FUTURE WORK

The simulation and mathematical results show that the presented class-E resonant inverter design offers high ECE and reasonable performance during load variation within a certain load region. Better load variation performance requires a lower Q_L and lower overall efficiency and output power capability. Load impedance for ZVS and ZDS conditions is unique and any load variation causes these conditions to be lost. Switch device internal resistance when less than 1.5 Ω has only substantial effect on the ECE and not load current or voltage. This concept establishes the reasonable assumption for the mathematical analysis to neglect the internal resistance of the switching device. Similar output power performance between the simulation and mathematical models were achieved. Discrepancies between these models were caused by the additional assumptions used in the mathematical model. These notable assumptions include neglecting the effects of the antiparallel diode intrinsic to Q_1, neglecting phase difference between I_O and V_O when calculating P_O, and assuming the load current consists of only the frequency of f_{SW} and not the two resonant frequencies f_{rCon} and f_{rCoff}. Experimental results showed minor comparison between the simulation and mathematical models. This was mainly due simulation and mathematical assumptions that did not consider parasitic effects and nonlinear shunt capacitance intrinsic to the utilized MOSFET and Schottky diode. Experimental results clearly show the two different resonant frequencies $f_{r,Con}$ and $f_{r,Coff}$ causing impurity and a DC offset of the load voltage waveform.

Future simulation and mathematical models should have the nonlinear shunt capacitance of the switching component and other parasitic impedances analyzed. In addition, the behavior of the resonant tank should be monitored and studied. These models would be very complex and involve high order differential equations. However, by having these advanced models made an

experimental test bed can be established which more closely resembles the simulation and mathematical models. Mathematical assumptions should not neglect a load current comprised of $f_{r,Con}$ and $f_{r,Coff}$. Experimental test beds should aim to select switching devices with a minimum amount of intrinsic capacitance to avoid nonlinear shunt capacitance.

REFERENCES

[1] O. C. Onar, S. L. Campbell, L. E. Seiber, C. P. White and M. Chinthavali, "A high-power wireless charging system development and integration for a Toyota RAV4 electric vehicle," 2016 IEEE Transportation Electrification Conference and Expo (ITEC), Dearborn, MI, 2016, pp. 1-8.

[2] R. Bosshard and J. W. Kolar, "Inductive power transfer for electric vehicle charging: Technical challenges and tradeoffs," in *IEEE Power Electronics Magazine*, vol. 3, no. 3, pp. 22-30, Sept. 2016.

[3] T. Nagashima *et al*., "Analytical design procedure for resonant inductively coupled wireless power transfer system with class-E2 DC-DC converter," *2014 IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne VIC, 2014, pp. 113-116.

[4] Z. N. Low, R. A. Chinga, R. Tseng and J. Lin, "Design and Test of a High-Power High-Efficiency Loosely Coupled Planar Wireless Power Transfer System," in *IEEE Transactions on Industrial Electronics*, vol. 56, no. 5, pp. 1801-1812, May 2009.

[5] S. Wang, F. Xue, A. Q. Huang and S. Liu, "Physics understanding of high temperature behavior of Gallium Nitride power transistor," 2016 IEEE 4th Workshop on Wide Bandgap Power Devices and Applications (WiPDA), Fayetteville, AR, USA, 2016, pp. 324-327.

[6] X. She; A. Q. Huang; O. Lucia; B. Ozpineci, "Review of Silicon Carbide Power Devices and Their Applications," in IEEE Transactions on Industrial Electronics, vol.PP, no.99, pp.1-1

[7] N. O. Sokal and A. D. Sokal, "Class E-A new class of high-efficiency tuned single-ended switching power amplifiers", IEEE Journal of Solid-State Circuits, vol. 10, no. 3, pp. 168-176, Jun 1975.

[8] M. Kazimierczuk and K. Puczko, "Exact analysis of class E tuned power amplifier at any Q and switch duty cycle," in *IEEE Transactions on Circuits and Systems*, vol. 34, no. 2, pp. 149-159, Feb 1987.

[9] Muhammad H. Rashid, "Power Electronics Circuit, Devices, and Applications", 4th Edition, Wiley, 2013.

[10] Y. C. Chuang, Y. L. Ke, H. S. Chuang and M. L. Chou, "Electronic Ballasts Driven by Hybrid Source Using Microprocessor-Controlled Digital Switching Technique," in IEEE Transactions on Industry Applications, vol. 47, no. 3, pp. 1452-1460, May-June 2011.

[11] G. D. Funk and R. H. Johnston, "A linearized 1 GHz class E amplifier," *Proceedings of the 39th Midwest Symposium on Circuits and Systems*, Ames, IA, 1996, pp. 1355-1358 vol.3.

[12] G. Notzon, T. Busch, M. van Delden and T. Musch, "A 500W high efficiency class-E power amplifier for heating a variable plasma load at 10MHz," *2016 German Microwave Conference (GeMiC)*, Bochum, 2016, pp. 429-432.

[13] I. Boonyaroonate and S. Mori, "Analysis and design of class E isolated DC/DC converter using class E low dv/dt PWM synchronous rectifier," in *IEEE Transactions on Power Electronics*, vol. 16, no. 4, pp. 514-521, Jul 2001.

[14] H. L. Cheng, C. A. Cheng, C. C. Fang and H. C. Yen, "Single-Switch High-Power-Factor Inverter Driving Piezoelectric Ceramic Transducer for Ultrasonic Cleaner," in *IEEE Transactions on Industrial Electronics*, vol. 58, no. 7, pp. 2898-2905, July 2011.

[15] C. Wang, L. E. Larson and P. M. Asbeck, "Improved design technique of a microwave class-E power amplifier with finite switching-on resistance," Radio and Wireless Conference, 2002. RAWCON 2002. IEEE, 2002, pp. 241-244.

[16]   T. Suetsugu and M. Kazimierczuk, "Analysis of transient behavior of class E amplifier due to load variations," Power Electronics and Drive Systems (PEDS), 2011 IEEE Ninth International Conference on, Singapore, 2011, pp. 600-603.

[17]   Z. N. Low, J. J. Casanova, P. H. Maier, J. A. Taylor, R. A. Chinga and J. Lin, "Method of Load/Fault Detection for Loosely Coupled Planar Wireless Power Transfer System With Power Delivery Tracking," in *IEEE Transactions on Industrial Electronics*, vol. 57, no. 4, pp. 1478-1486, April 2010.

[18]   M. K. Kazimierczuk, J. Jozwik, "Resonant DC/DC converter with class-E inverter and class-E rectifier", IEEE Transactions on Industrial Electronics, Vol.36, Iss. 4, pp: 468 – 478, 1989.

[19]   T. Nagashima, X. Wei, H. Sekiya, "Analytical design procedure for resonant inductively coupled wireless power transfer system with class-DE inverter and class-E rectifier", 2014 IEEE Asia Pacific Conference on Circuits and Systems (APCCAS), pp:288 – 291, Ishigaki, Japan, 2014.

[20]   J. M. Rivas, Y. Han, O. Leitermann, A. Sagneri, and D. J. Perreault, "A High-Frequency Resonant Inverter Topology with Low Voltage Stress", IEEE Transactions on Power Electronics, Vol. 23, No. 4, pp: 1759-1771, July 2008.

[21]   R. Frey, "500 W, class E 27.12 MHz amplifier using a single plastic MOSFET," Advanced Power Technology Application Note APT9903, 1999, Advanced Power Technology, Bend, OR, 1999.

[22]   P. Jain, M. Pahlevaninezhad, S. Pan and J. Drobnik, "A Review of High-Frequency Power Distribution Systems: For Space, Telecommunication, and Computer Applications," in IEEE Transactions on Power Electronics, vol. 29, no. 8, pp. 3852-3863, Aug. 2014.

[23]   T. Suetsugu and M. Kazimierczuk, "Steady-state behavior of class E amplifier outside designed conditions," 2005 IEEE International Symposium on Circuits and Systems, 2005, pp. 708-711 Vol. 1.

[24]   T. Nagashima, X. Wei, T. Suetsugu, M. K. Kazimierczuk and H. Sekiya, "Waveform Equations, Output Power, and Power Conversion Efficiency for Class-E Inverter Outside Nominal Operation," in IEEE Transactions on Industrial Electronics, vol. 61, no. 4, pp. 1799-1810, April 2014.

[25]   T. Nagashima, X. Wei, H. Sekiya and M. K. Kazimierczuk, "Power conversion efficiency of class-E power amplifier outside nominal operation," *2011 IEEE International Symposium of Circuits and Systems (ISCAS)*, Rio de Janeiro, 2011, pp. 749-752.

[26]   M. Acar, A. J. Annema and B. Nauta, "Analytical Design Equations for Class-E Power Amplifiers with Finite DC-Feed Inductance and Switch On-Resistance," 2007 IEEE International Symposium on Circuits and Systems, New Orleans, LA, 2007, pp. 2818-2821.

[27]   F. Raab, "Idealized operation of the class E tuned power amplifier," in IEEE Transactions on Circuits and Systems, vol. 24, no. 12, pp. 725-735, Dec 1977.

[28]   M. Acar, A. J. Annema and B. Nauta, "Generalized Design Equations for Class-E Power Amplifiers with Finite DC Feed Inductance," *2006 European Microwave Conference*, Manchester, 2006, pp. 1308-1311.

[29]   D. J. Kessler and M. K. Kazimierczuk, "Power losses and efficiency of class-E power amplifier at any duty ratio," in IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 51, no. 9, pp. 1675-1689, Sept. 2004.

[30]   M. Albulet and R. E. Zulinski, "Effect of switch duty ratio on the performance of class E amplifiers and frequency multipliers," in IEEE Transactions on Circuits and Systems I: Fundamental Theory and Applications, vol. 45, no. 4, pp. 325-335, Apr 1998.

APPENDIXES

A. EXPERIMENT HARDWARE SETUP

The bill of material for purchasing parts used on the PCB are shown in Table 10. Various capacitors and an adjustable inductor were purchased to allow different experiments outlined in Table 9.

Table 10 Bill of material for test bed

Component	Quantity	MFG Part Number	Manufacturer
Capacitor	2	DEHR33F181KC3B	Murata Electronics North America
Capacitor	5	DEA1X3F101JA3B	Murata Electronics North America
Capacitor	2	DEA1X3F470JC3B	Murata Electronics North America
Capacitor	1	DEA1X3F390JC3B	Murata Electronics North America
Capacitor	2	DEA1X3F330JC3B	Murata Electronics North America
Capacitor	1	DEA1X3F270JC3B	Murata Electronics North America
Capacitor	1	DEA1X3F180JCDB	Murata Electronics North America
Capacitor	3	DEA1X3F150JCDB	Murata Electronics North America
Capacitor	1	DEA1X3F220JCDB	Murata Electronics North America
Capacitor	3	DEA1X3F100JCDB	Murata Electronics North America
E Type Magnetic Core	1	0F43007EC	Magnetics Inc.
MOSFET	2	C2M0280120D	CREE
Choke Inductor	1	AIRD-03-152K	Abracon LLC
Driver	1	FAN3111ESX	Fairchild Semiconductor
DB9 Connector	1	A-DF-09-A/KG-T2S	Assmann WSW Components
Two Position Terminal Block	2	1776275-2	TE Connectivity AMP Connectors
Load Resistance	2	PF2472-200RF1	Riedon
Load Resistance	2	PF2472-100RF1	Riedon
Load Resistance	2	PF2472-50RF1	Riedon

LED Diode	1	5501304F	Dialight
LED Resistor	1	CMF55102K00FHEB	Vishay Dale
Fuse	1	BK/PCE-5-R	Eaton
Schottky Diode	1	GP2D005A120A	Global Power Technologies Group
Hex Stand Off	1	25505	Keystone Electronics
Nut for Hex Stand Off	1	4688	Keystone Electronics

CadSoft Eagle Professional 7.6.0 software was used to design the PCB using the components from Table 10. The Eagle CAD schematic file (Figure 28) was used to generate the board file (Figure 29). The CAM Processor feature of the Eagle software was used to generate files from the board file that could be transferred to gerber files using the GerberLogix software. These gerber files were sent to and used by a local manufacturer to create the PCB.

The inductor, L, was custom constructed by turning magnetic core wire around a type E magnetic core using manufacturer of the magnetic cores guidelines for design. A LCR meter was used to validate passive inductor and capacitor elements met manufacturer listings. A multimeter was used to validate resistor values met manufacturer listings. A waveform test circuit was constructed to validate the performance of the MOSFET.

Signals identified in the schematic (Figure 28) are identified in Table 11. A high power AC to DC power supply was used to provide the supply voltage. A traditional lab DC power supply was used to supply the input and reference voltages for the driver circuit. For all experiments listed in Table 9 an input voltage of +12 V and a reference voltage of +3 V was used for the gate driver. A function generator was used to provide the square wave pulse width modulation (PWM) signal to the gate driver. For all experiments listed in Table 9 the amplitude of the PWM signal was +/- 3 V. The PCB (Figure 29) consists of two layers including the top layer for control and power and the bottom layer for grounding. At higher frequencies parasitic impedance noise becomes more problematic for design. Components were spaced as closely as
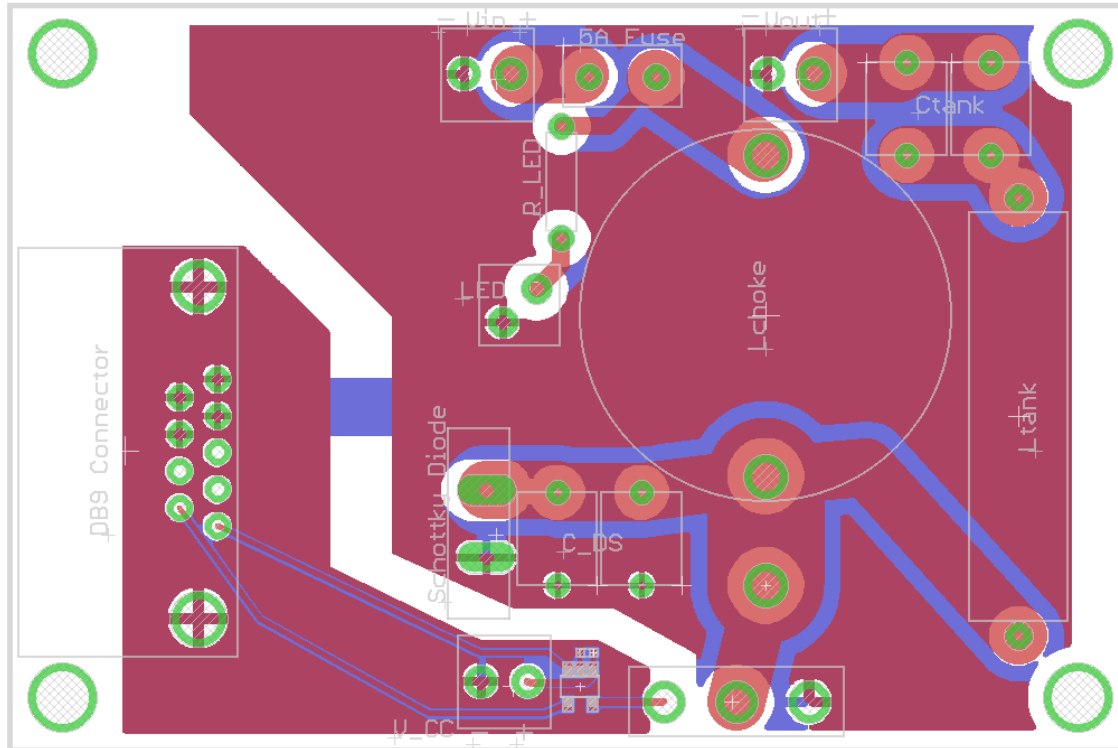
possible on the PCB to reduce the effects of parasitic noise. The top layer area was maximized while allowing power connections to reduce the electromagnetic interference related to high frequency switching operation.

Figure 28 Eagle CAD PCB schematic

Table 11 Signal list for schematic in Figure 28

Signal	Function
U$10G$1	+ Supply Voltage
U$10G$2	- Supply Voltage
U$17G$1	+ VREF
U$17G$2	- VREF
P$1	+ PWM
P$6	- PWM

Figure 29 Eagle CAD two layer PCB board file

VITA

Richard Jennings is a student member of IEEE. He graduated Summa Cum Laude from the West Virginia University with the Bachelor of Science degree in electrical engineering in December 2012. Following his graduation he was employed at Huntington Ingalls as an electrical engineer responsible for retrofitting electric power systems on maritime vessels until June 2016. From June 2016 to present he has been employed as an electrical engineer at ABB where he is responsible for the power electronics design of traction converters. Richard began his master studies at Old Dominion University concurrent to his full time employment in May 2013 and will graduate with the Master of Science degree in electrical and computer engineering in May 2017.