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FABRICATION OF NMOS LOGIC GATES

by

Samantha Hahn
B.S. May 2019, Old Dominion University

A Thesis Submitted to the Faculty of Old Dominion University in the Partial Fulfillment of the Requirements for the Degree of

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ENGINEERING - ELECTRICAL AND COMPUTER

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May 2022

Approved by:

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ABSTRACT

FABRICATION OF NMOS LOGIC GATES

Samantha Hahn
Old Dominion University, 2022
Director: Dr. Sylvain Marsillac

NMOS logic gates were a predecessor to the CMOS logic gates widely used today. They allow for easier process steps and take into account the limited equipment that is available in the ODU clean room. In this thesis, NMOS logic gates were studied in order to open a new field of research into logic gates at Old Dominion University. This work focuses mostly on the designs of the mask patterns and the design of the fabrication process. NOT, NOR, NAND, OR, and AND gates were fabricated with transistors with a 75 μm gate length, using masks and processes specifically developed for our equipment, such as the maskless mask aligner. All gates fabricated demonstrated the expected behavior but with some limitations. Due to a high value on the on resistance for the transistor (R_{on}), the voltage divider between the on and off state of the transistor is not as distinguishable as in our simulations. This leads to a voltage range for the LOW or HIGH outputs to be narrower than anticipated, at 0 to 3 V and 3 to 4 V respectively. Future designs of the NMOS logic gates should work towards reducing the R_{on} value.

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This thesis is dedicated to those who wish to peek inside the black box.

ACKNOWLEDGMENTS

I would never have been able to finish writing my thesis without several, incredibly patient, kind, and supportive people in my life. I would like to thank my advisor, Dr. Sylvain Marsillac, for all his guidance and encouragement throughout the work on this thesis. When I got lost in a maze of details, he was there to remind me to stop overthinking and to re-focus me so that I could get back on track. I would also like to thank my colleagues, Ben Belfore and Adam Masters for their invaluable assistance in the lab and particularly for being able to bounce ideas off of Adam. Further, I would like to thank my dad and my significant other, Arthur Wiedemann, for their support, patience, and encouragement during trying times.

NOMENCLATURE

CMOS	Complimentary Moss
$((CH_3)_2CO)$	Acetone
CH_3COOH	Acetic Acid
C_{ox}	Capacitance of Oxide Layer
DI	Deionized
DIBL	Drain Induced Barrier, mV/V
DMM	Digital Multimeter
HF	Hydrofluoric Acid
H_2O_2	Hydrogen Peroxide
H_2SO_4	Sulfuric Acid
HNO_3	Nitric Acid
H_3PO_4	Phosphoric Acid
I	Current, A
I_{off}	Off Current, A
I_{on}	On Current, A
L	Length of Channel, μm
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
NMOS	N-channel MOSFET
PR	Photoresist
+PR	Positive Photoresist
-PR	Negative Photoresist
PTFE	Polytetrafluoroethylene
r_d	Output Resistance, Ω
R_{off}	Off Resistance, Ω
R_{on}	On Resistance, Ω
R_R	Resistor Resistance, Ω
R_{trans}	Resistance Due to Transistor(s), Ω
SS	Subthreshold Swing
V	Voltage, V
V_{DD}	Voltage Supply, V
V_{DS}	Drain to Source Voltage, V
$V_{DS\ max}$	Maximum Drain to Source Voltage, V
V_{DSsat}	Drain to Source Saturation Voltage, V
V_{GS}	Gate to Source Voltage, V
V_{out}	Output Voltage, V
V_{OV}	Overdrive Voltage, V
V_t	Threshold Voltage, V
V_{tlin}	Threshold Voltage in the Linear Region, V
V_{tsat}	Threshold Voltage in the Saturation Region, V
W	Width of Channel, μm
μ_n	Electron Mobility, m^2/V-s

TABLE OF CONTENTS

Page

LIST OF TABLES viii
LIST OF FIGURES ix
CHAPTER 1. INTRODUCTION 1
1.1 Background 1
1.2 How NMOS Transistors Work 3
CHAPTER 2. SIMULATIONS 7
2.1 Circuit Configurations 7
2.2 Resistor Values 29
CHAPTER 3. FABRICATION 31
3.1 Substrate Preparation 32
3.2 Oxidation 33
3.3 Photolithography for the Diffusion Window 36
3.4 Oxide Etch for Diffusion Window 39
3.5 Strip Photoresist 39
3.6 Pre-deposition 39
3.7 Drive-In and Oxidation 41
3.8 Photolithography for Metal Contact Windows 42
3.9 Oxide Etch for Metal Contact Windows 42
3.10 Strip Photoresist 42
3.11 Metallization 42
3.12 Photolithography for Metal Contacts 44
3.13 Metal Etch 45
3.14 Strip Photoresist 45
CHAPTER 4. GATE DESIGN AND CHARACTERIZATION RESULTS 46
4.1 Gate Layout Designs 46
4.2 Transistor Parameters 54
4.3 Logic Gates 60
4.3.1 NOT Gate Wafer Characterization 60
4.3.2 Other Logic Gates tested with 75 μm Gate 66
CHAPTER 5. CONCLUSION 72
REFERENCES 73

LIST OF TABLES

Table Page

Table 1: NOT Gate Truth Table.. 8
Table 2: NOR Gate Truth Table 10
Table 3: NAND Gate Truth Table 15
Table 4: OR Gate Truth Table 20
Table 5: AND Gate Truth Table 25

LIST OF FIGURES

Figure Page

Figure 1: Logic gate symbols and their corresponding truth tables. 2
Figure 2: Regions of an IV curve representing different modes of operation. 6
Figure 3: NOT Gate Circuit Simulation. 7
Figure 4: NOT Gate Circuit Voltages when T_1 is low. 8
Figure 5: NOT Gate Circuit Voltages when T_1 is high. 9
Figure 6: NOR Gate Circuit Simulation 10
Figure 7: NOR Gate Circuit Voltages when T_1 and T_2 are low. 11
Figure 8: NOR Gate Circuit Voltages when T_1 is low and T_2 is high. 12
Figure 9: NOR Gate Circuit Voltages when T_1 is high and T_2 is low. 13
Figure 10: NOR Gate Circuit Voltages when T_1 and T_2 are high. 14
Figure 11: NAND Gate Circuit Simulation 15
Figure 12: NAND Gate Circuit Voltages when T_1 and T_2 are low. 16
Figure 13: NAND Gate Circuit Voltages when T_1 is low and T_2 is high. 17
Figure 14: NAND Gate Circuit Voltages when T_1 is high and T_2 is low. 18
Figure 15: NAND Gate Circuit Voltages when T_1 and T_2 are high. 19
Figure 16: OR Gate Circuit Simulation 20
Figure 17: OR Gate Circuit Voltages when T_1 and T_2 are low. 21
Figure 18: OR Gate Circuit Voltages when T_1 is low and T_2 is high. 22
Figure 19: OR Gate Circuit Voltages when T_1 is high and T_2 is low. 23
Figure 20: OR Gate Circuit Voltages when T_1 and T_2 are high. 24
Figure 21: AND Gate Circuit Simulation 25
Figure 22: AND Gate Circuit Voltages when T_1 and T_2 are low. 26
Figure 23: AND Gate Circuit Voltages when T_1 is low and T_2 is high. 27
Figure 24: AND Gate Circuit Voltages when T_1 is high and T_2 is low. 28
Figure 25: AND Gate Circuit Voltages when T_1 and T_2 are high. 29
Figure 26: Step processes for the fabrication of the NMOS. Figure is not to scale. 32
Figure 27: The oxidation furnace Lindberg Moldatherm Hinged Tube Furnace 55647. 35
Figure 28: Photo of the µMLA Maskless Aligner by Heidelberg Instruments for the alignment and exposure system. 38
Figure 29: The pre-deposition furnace is the Thermco mini-brute diffusion furnace (Model MB-80H). 40
Figure 30: Schematic showing the effect of gate oxide on the electric field. The orange region represents the electric field, the yellow regions represent the doped regions, the blue regions represent the dielectric, and the gray regions represent the metal regions. The areas within the red circles note areas of interest. 41
Figure 31: The electron beam that deposits aluminum is a KJL PVD 75. 43
Figure 32: KLayout design featuring various transistor channel lengths (200 µm, 150 µm, 100 µm, and 75 µm) and resistor combinations. 47
Figure 33: Close up of inverter with gate length of 200 µm paired with the largest resistor. 48
Figure 34: KLayout design featuring NOT, NOR, NAND, OR, and AND gates. 49

Figure 35: Close-up of the layout featuring the NOR gate with channel length of 75 µm........... 50
Figure 36: Close-up of the layout featuring the NAND gate with channel length of 75 µm. 51
Figure 37: Close-up of the layout featuring the OR gate with channel length of 75 µm. 52
Figure 38: Close-up of the layout featuring the AND gate with channel length of 75 µm. 53
Figure 39: Illustration of the length and width of a typical transistor used in this work. 54
Figure 40: Set-up used to measure the transistor characteristics. 55
Figure 41: Close-up of the set-up used to measure the transistor characteristics. 56
Figure 42: Typical I-V characteristics measured for a transistor used in this work. 56
Figure 43: Typical transfer characteristics of a transistor used in this work. 57
Figure 44: Graph illustrating the extraction of r_d and R_{on} from the data. The blue line is the original data, the orange line is a curve fitted line that is used to find r_d, and the yellow line is a curve fitted line that is used to find R_{on}. 58
Figure 45: Graph illustrating the extraction of the threshold voltage from the data.................... 59
Figure 46: Graph illustrating the extraction DIBL from the data. 60
Figure 47: Hardware setup for characterizing the NOT gates. An extra pair of probes resting on improvised mounts were connected to a DMM to measure V_{DS}. 62
Figure 48: I_{DS} vs V_{DS} graph for the NOT gate with a channel length of 200 µm and the largest resistor. 63
Figure 49: VTC graph for the NOT gate with channel length of 200 µm and largest resistor. 63
Figure 50: I_{DS} vs V_{DS} graph for the NOT gate with a channel length of 75 µm and the largest resistor. 64
Figure 51: VTC graph for the NOT gate with channel length of 75 µm the largest resistor. 64
Figure 52: A typical VTC graph for a NOT gate [4]. 65
Figure 53: The I-V characteristic for the resistor used. 66
Figure 54: The IV characteristic for the resistor. 68
Figure 55: The IV Characteristic of the NOR gate with the 01 input. 69
Figure 56: The IV Characteristic of the NOR gate with the effective 00 input. 70

CHAPTER 1. INTRODUCTION

1.1 Background

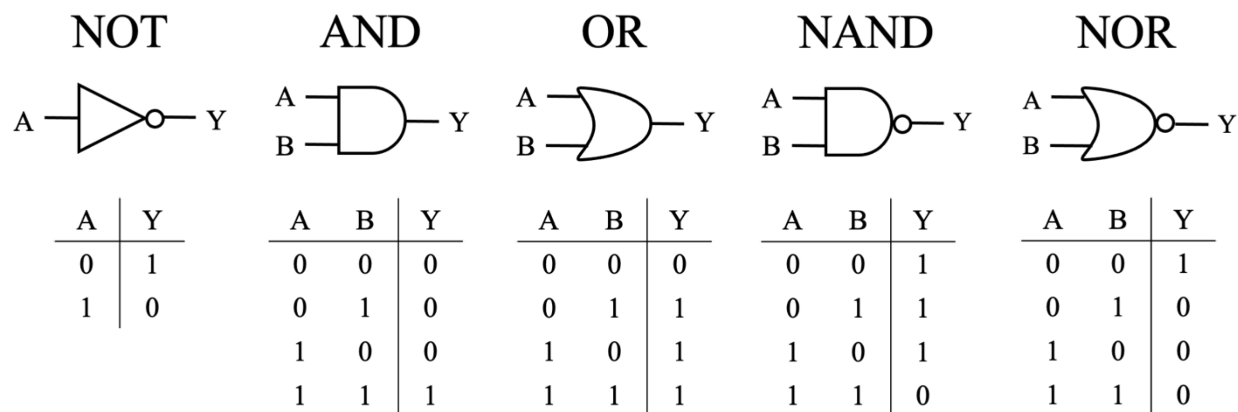
Logic gates are the building blocks for the fabrication of integrated circuits and are therefore key for computers performance. A logic gate is a digital circuit where the configuration of the devices produces a particular output based on one or more particular inputs [1]. Since logic gates are digital circuits, the input and output signals operate at discrete voltages where the voltages take on a finite number of values [1], [2]. Usually, 0 volts (V) represents a Logic 0, and some other non-zero voltage represents a Logic 1 [1]. Logic 0 signals may also be referred to as just 0, False, or Low [1]. Likewise, Logic 1 signals may be referred to as just 1, True, or High [1]. Since there are only two values a signal can take, either a Logic 0 or a Logic 1, the system is binary [1].

The p-n junction was invented by Shockley in 1949 [3]. P-N junctions are important in the design and application in a variety of devices such as some types of diodes, the thyristor, and the Bipolar Junction Transistor (BJT) [3], [4]. Avalanche diodes prevent high voltages from destroying circuits [5], photodiodes generate electricity from light, Light Emitting Diodes (LEDs) generate light from electricity, and varactors tune radio receivers [4]. The thyristor is used in high voltage and high current switching applications [3]. BJTs have many uses including amplifiers, converters, temperature sensors, clipping waveforms, and high frequency operation [6]. P-N junctions are also part of the design of the Metal Oxide Semiconductor Field Effect Transistor (MOSFET) [4]. The MOSFET was invented by Kahng and Atalla in 1960 [3]. Logic gates are made of MOSFETS, with either a n-type channel (NMOS) or a p-type channel (PMOS) [4]. The popular Transistor-Transistor Logic (TTL) family was comprised of BJTs and would be replaced by NMOS logic in the 1980s due to the amount of transistors increasing on the chip and power dissipation [4]. The Complimentary MOS (CMOS) logic comprising of both NMOS and PMOS

transistors replaced the NMOS logic for the same reasons NMOS logic replaced TTL logic [4]. Due to limitations in lab equipment, this thesis focuses on NMOS logic.

Some of the most basic gates include NOT (also known as an inverter), NAND, and NOR. Some composite gates include AND and OR. Their symbols and corresponding truth tables are shown in Figure 1 [1]. A truth table shows the inputs with their corresponding outputs. A and B are the inputs and Y is the output. The NOT gate has only one input, and its output is the opposite of its input.

The rest of the gates must have at least two inputs. When both of the AND gate's inputs are High, the output is High. When either or both of the OR gate's inputs are High, the output is High. When neither or either, but not both, of the NAND gate's inputs are High, then the output is High. Another way to look at it is when both of the NAND gate's inputs are High, the output is Low. When both of the NOR gate's inputs are Low, the output is HIGH.



NOT

A	Y
0	1
1	0

AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

NAND

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Figure 1: Logic gate symbols and their corresponding truth tables.

The purpose of this thesis is to open a new area of research at Old Dominion University by developing a fabrication system for NMOS logic gates as a steppingstone for CMOS logic gates, which are widely used in today's technology. NMOS logic gates were fabricated rather than

CMOS logic gates due to a limitation in lab equipment. CMOS logic gates require two pre-deposition furnaces for n and p-type dopants to prevent cross-contamination. The lab only has one pre-deposition furnace, and thus only NMOS logic gates were made. Another limitation included a lack of Chemical Vapor Deposition equipment in order to deposit high quality contacts made of polysilicon. Thus, Physical Vapor Deposition through the use of an electron beam (e-beam) was used to apply aluminum as the metal contacts. Before this thesis, only isolated devices were fabricated. Through the work of this thesis, devices were connected together to form the basis of an integrated circuit.

1.2 How NMOS Transistors Work

A transistor is a device that has at least three terminals, and one terminal controls the amount of current flowing between the other two terminals [7], [4]. One of the most common and important types of transistors is the metal-oxide-semiconductor field-effect transistor (MOSFET) [7], [4]. This section explains how an n-channel MOSFET (NMOS) in enhancement mode works.

The NMOS has a semiconductor substrate that is doped as p-type [4]. Within the substrate are two regions that are heavily doped as n-type [4]. These n-type regions are known as the source and drain [4]. An oxide layer lies on top of the semiconductor substrate and between the source and drain [4]. A metal contact lies on top of the oxide, which represents the gate terminal [4]. Separate metal contacts also lie on top the source and drain regions to create the source and drain terminals [4]. Since the source, substrate, and drain essentially create two diodes that oppose each other, current is unable to flow [4].

For the moment, consider the source and drain to be grounded while a positive voltage is applied to the gate [4]. In the region of the substrate that is near the gate oxide, the positive gate voltage pushes the holes away so that they move further down in the substrate [4]. The acceptor

atoms in the region of the substrate that is near the gate oxide now have a negative charge and are thus ionized, and a depletion region is formed due to the lack of free moving carriers [4]. As the gate voltage increases, electrons from the source and drain are attracted towards the surface of the substrate that is underneath the gate oxide [4]. So the surface originally had majority carriers as holes, then the holes were depleted, and then mobile electrons accumulated at the surface, so the majority carriers became electrons. Thus, the surface type is inverted from p-type to n-type. When the concentration of electrons is less than the concentration of holes in the bulk of the semiconductor, the surface is weakly inverted [3]. When the concentration of electrons is higher than holes in the bulk of the semiconductor, the surface is strongly inverted [3]. When the gate voltage is large enough to attract enough electrons to strongly invert the surface of the substrate, a channel of electrons connects the source to the drain, allowing electrons to move between the source and drain [4]. Since the channel is the induced n-type region, it is called an n-channel. The N in NMOS denotes the type of the channel in the MOSFET [4]. The amount of gate-to-source voltage, V_{GS}, takes to strongly invert the surface of the substrate and thus form a channel is called the threshold voltage, V_t [4]. When the V_{GS} applied is larger than V_t, the extra voltage is called the overdrive voltage, V_{OV} [4]. In the absence of voltage between the drain and the source, at $V_{DS} = 0$, there is no change of voltage along the channel, and the voltage across the oxide is uniformly applied.

Now that the mobile electrons can travel between the n-type regions, an electric field must push the mobile electrons in a particular direction so that current may flow [4]. Consider the source to be grounded, a positive V_{GS} that is larger than V_t is applied, and a small positive V_{DS} is applied. Electrons are attracted to the positive voltage at the drain, so electrons move from the source to the drain [4]. Since charged particles are moving, current is flowing. Equation (1.1) describes how

the current from drain to source is calculated [4]. I is the current, μ_n is the electron mobility, C_{ox} is the capacitance of the oxide layer, W is the width of the channel, L is the length of the channel or the distance between the highly doped n regions, V_{GS} is the gate-to-source voltage, and V_{DS} is the drain-to-source voltage [4].

$$I = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_t) V_{DS} \qquad (1.1)$$

Now consider the source is still grounded, and a positive V_{GS} that is larger than V_t is still applied and kept constant, but the amount of V_{DS} increases. Since V_{DS} is applied along the entire length of the channel, there is a change of voltage compared the source, from zero to V_{DS}. There is therefore a difference between the voltage applied between the gate and elements in the channel and therefore a variation in channel depth. This yields a tapering of the channel, with the side next to the drain is the shallowest. As the voltage between source and drain is increased, the channel is even more tapered, leading to increasing resistance. This ultimately leads to the typical I_{DS} versus V_{DS} characteristics, with a saturation in the current as V_{DS} increases [4]. Equation (1.2) describes how the current from drain to source is calculated when V_{DS} is less than V_{OV} [4]. I is the current, μ_n is the electron mobility, Cox is the capacitance of the oxide layer, W is the width of the channel, L is the length of the channel or the distance between the highly doped n regions, V_{GS} is the gate-to-source voltage, and V_{DS} is the drain-to-source voltage [4].

$$I = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_t) V_{DS} - \frac{1}{2} V_{DS}^2 \right] \qquad (1.2)$$

Now consider the case where V_{DS} increases so that it is equal to V_{OV}. When $V_{DS} = V_{OV}$, it has reached the saturation voltage, V_{DSsat}, where the current begins to stay constant despite any increase in V_{DS}. The end of the channel closer to the drain pinches off. A large electric field moves the few mobile charges at the pinched end of the channel very fast to the drain region [8]. As V_{DS} increases so that it is larger than V_{OV}, the remaining portion of V_{DS} that is excess of V_{OV} is “a

voltage drop across the depletion region [4]." Equation (1.3) describes how the current from drain to source is calculated when $V_{DS} \geq V_{OV}$ [4].

$$I = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 \qquad (1.3)$$

The following graph shows each mode of operation for Equations (1.1), (1.2), and (1.3). The region in pink represents Equation (1.1), the region in blue represents Equation (1.2), and the region in green represents Equation (1.3).

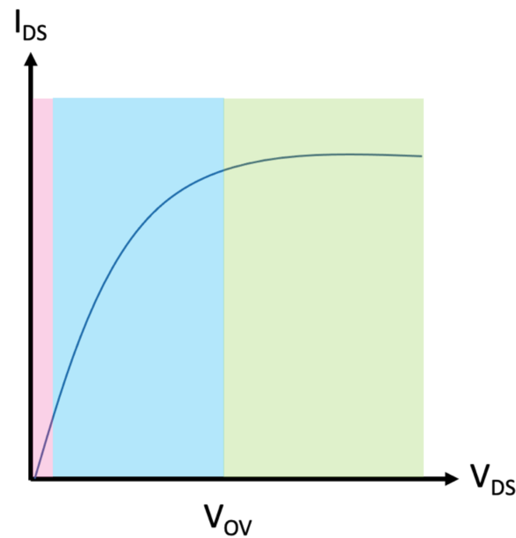


Figure 2: Regions of an IV curve representing different modes of operation.

CHAPTER 2. SIMULATIONS

2.1 Circuit Configurations

The program I used for my simulations was Simulink®. The circuit's voltage source, V_{DD}, is always 5 V. The gate voltage, V_G, for transistors Q_1 and Q_2 are 0 V when they are turned off and 5 V when they are turned on. The output voltage, V_{Out}, is always either 0 V or 5 V, depending on which transistors are on or off. V_{Out} also represents the output, F, on the truth table. On the truth table, 0 V is represented as 0 and 5 V is represented as 1. When something is turned off or has the value 0 on the truth table, it may also be called "low." When something is turned on or has the value 1 on the truth table, it may be called "high." The voltage results for all the simulations matched their respective truth tables.

The schematic used to test the inverter, or NOT gate, in Simulink® is shown in Figure 3. The truth table for the NOT gate is shown in Table 1. The results for the simulation are shown in Figures 4 and 5. In order to have a visible graph, the system had to be turned on for a period of time.

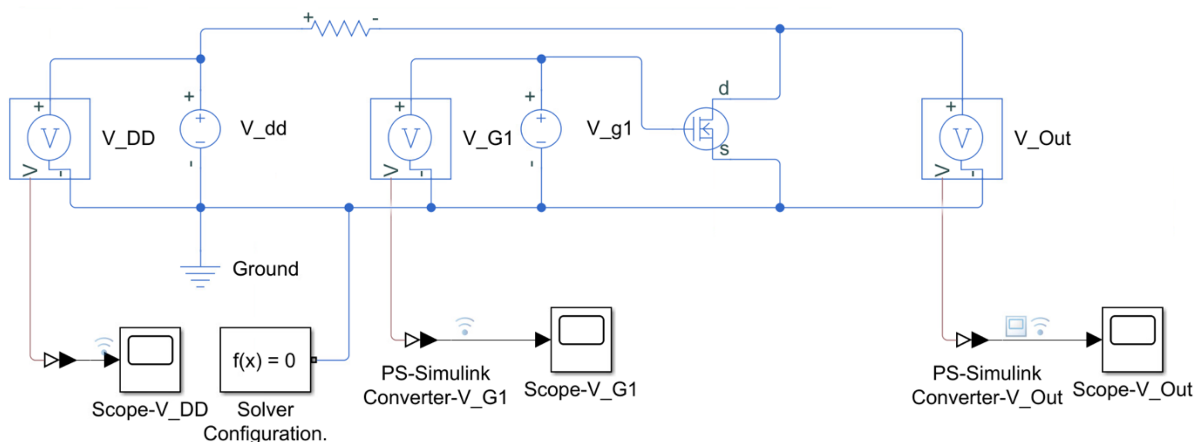


Figure 3: NOT Gate Circuit Simulation

Table 1: NOT Gate Truth Table

T_1	F
0	1
1	0

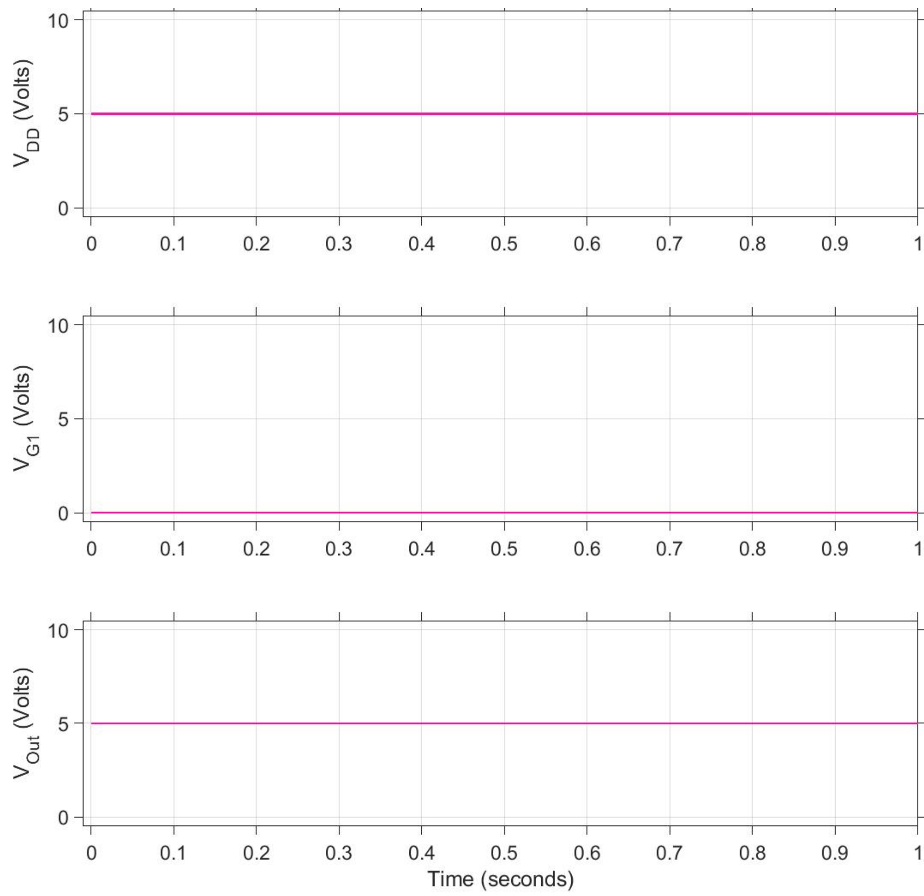


Figure 4: NOT Gate Circuit Voltages when T_1 is low.

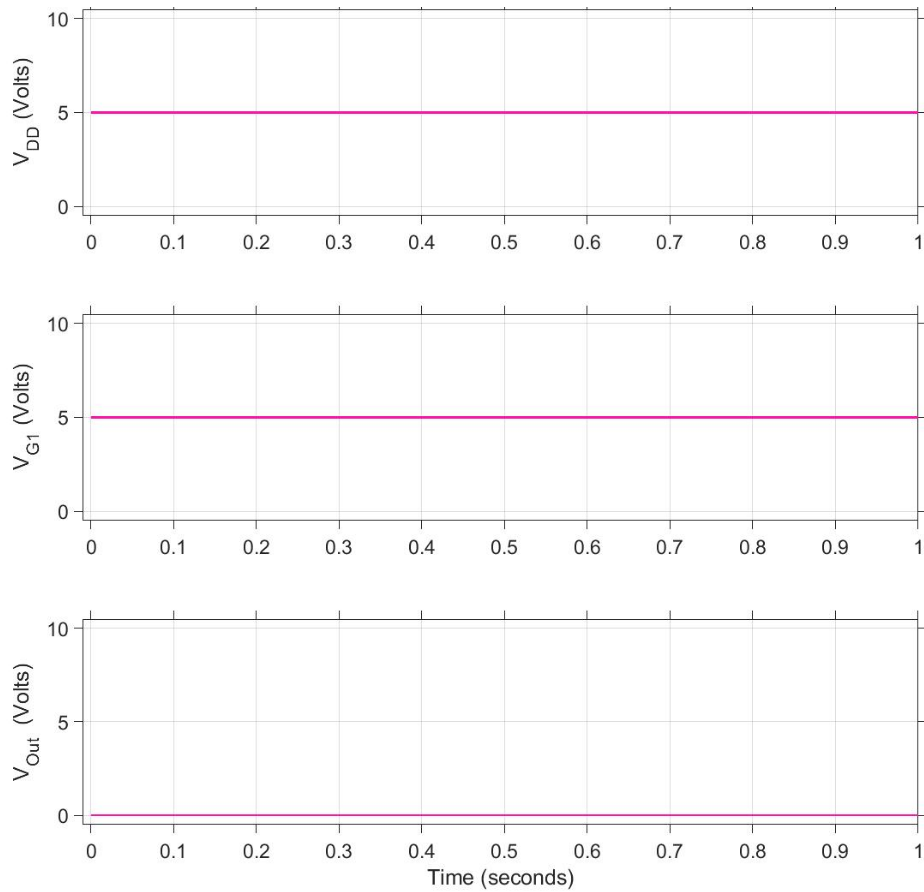


Figure 5: NOT Gate Circuit Voltages when T_1 is high.

The schematic used to test the NOR gate in Simulink® is shown in Figure 6. The truth table for the NOR gate is Table 2. The results for the simulation are shown in Figures 7 to 10.

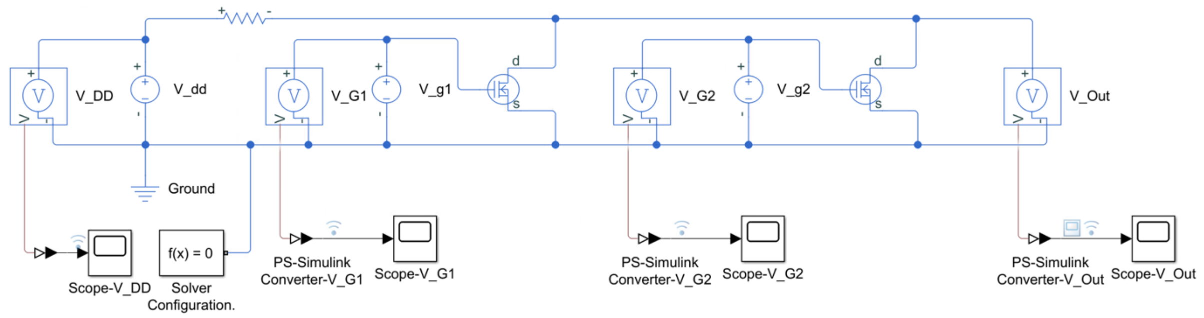


Figure 6: NOR Gate Circuit Simulation

Table 2: NOR Gate Truth Table

T_1	T_2	F
0	0	1
0	1	0
1	0	0
1	1	0

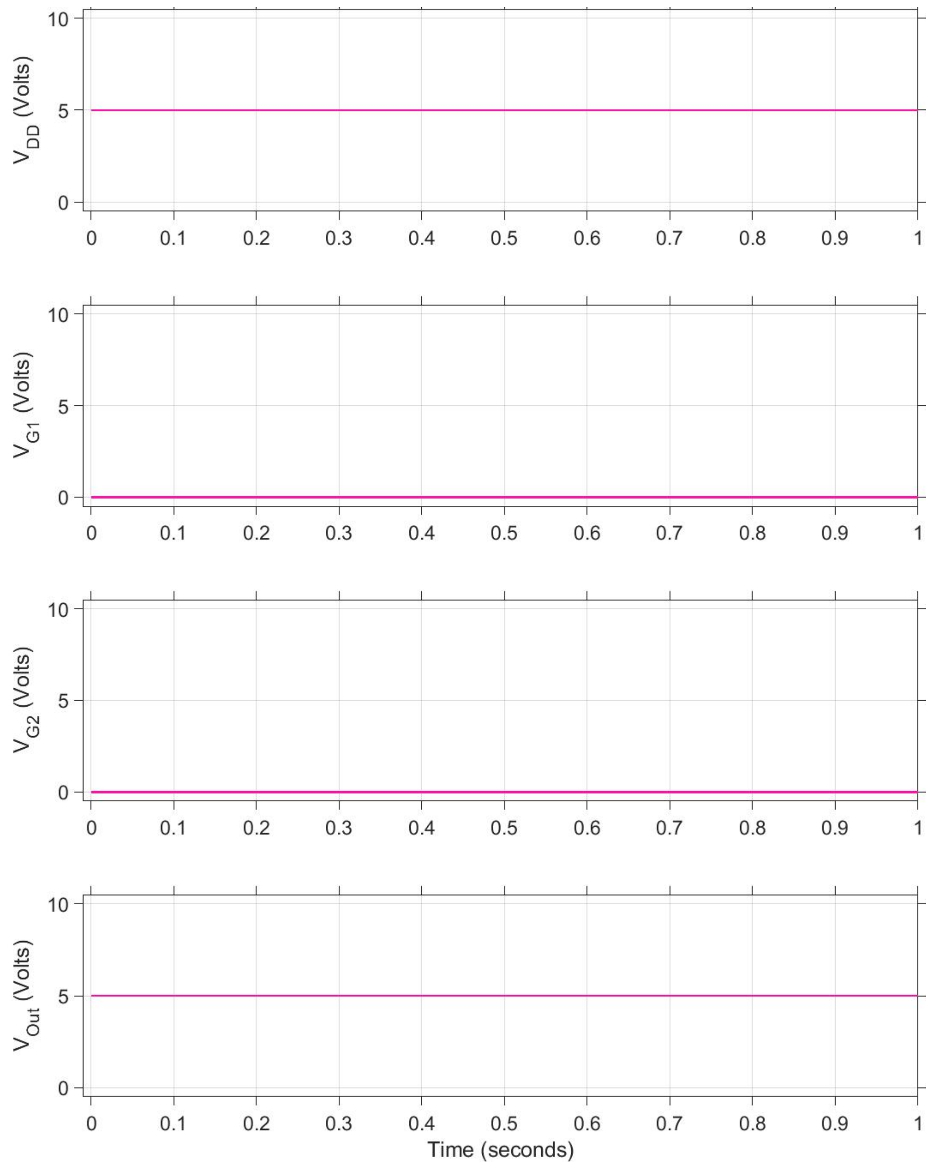


Figure 7: NOR Gate Circuit Voltages when T_1 and T_2 are low.

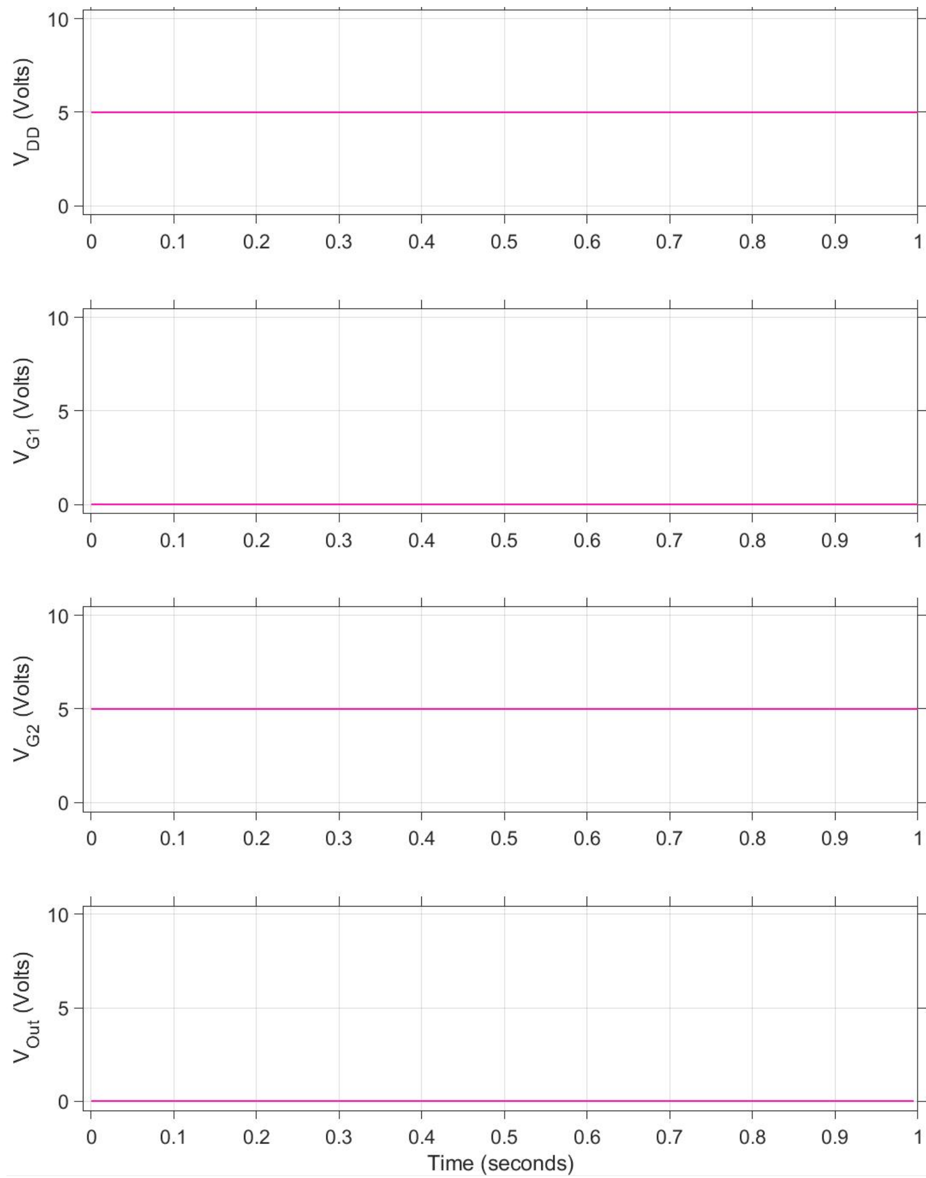


Figure 8: NOR Gate Circuit Voltages when T_1 is low and T_2 is high.

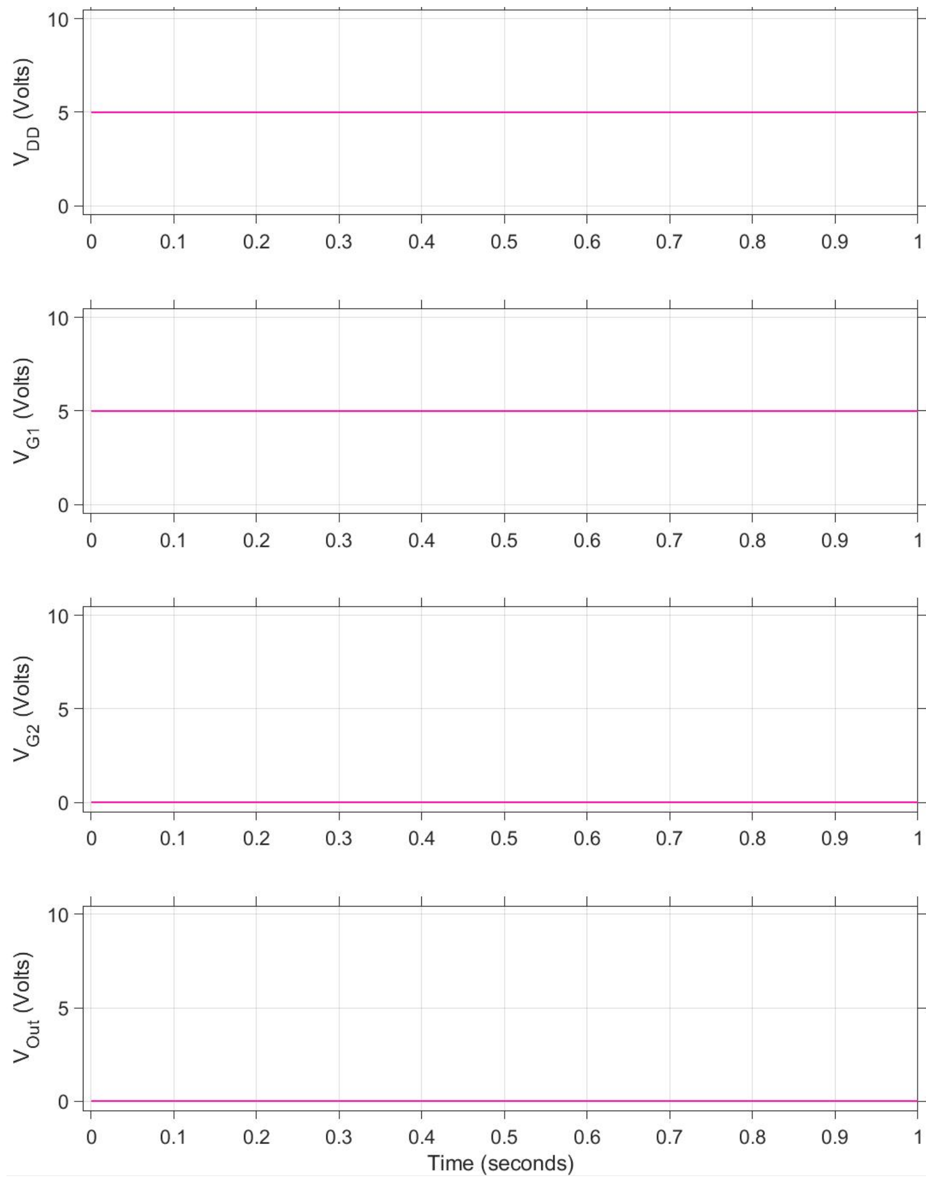


Figure 9: NOR Gate Circuit Voltages when T_1 is high and T_2 is low.

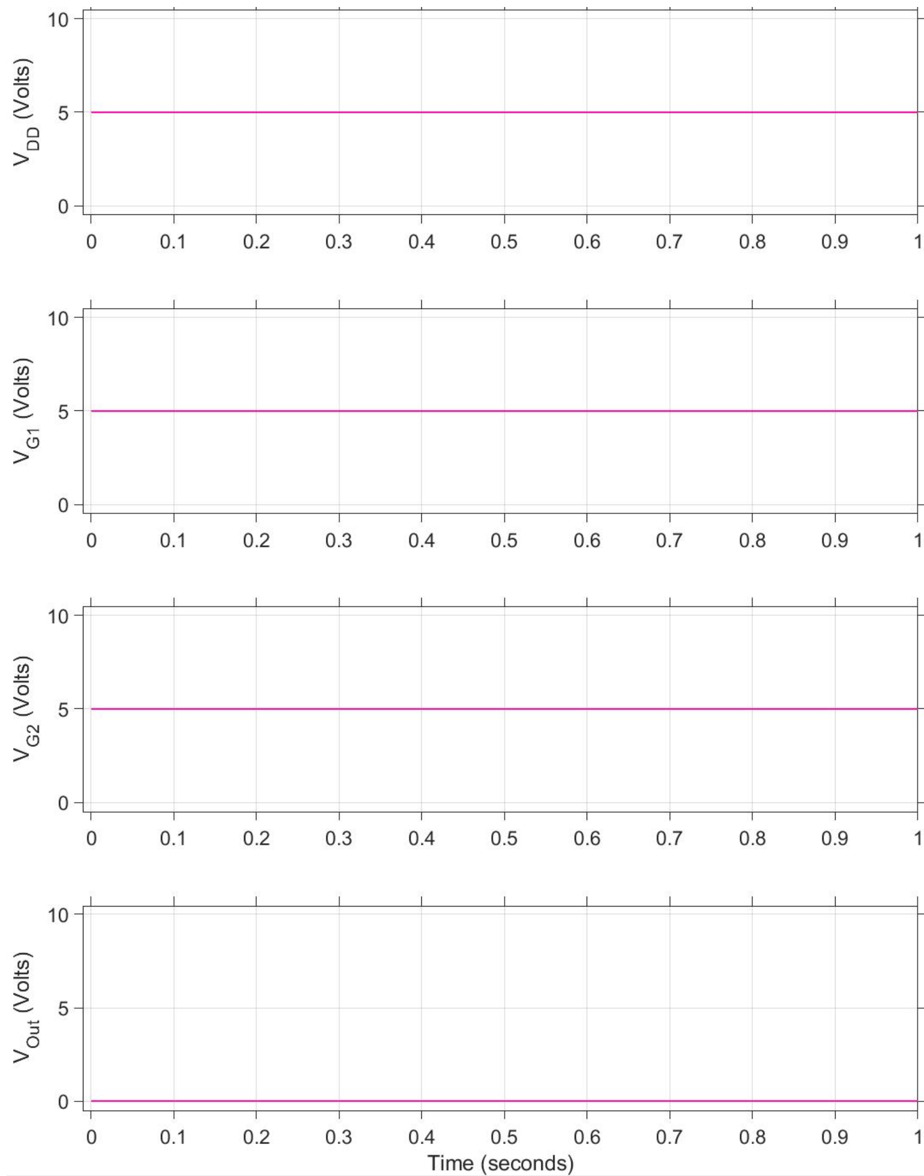


Figure 10: NOR Gate Circuit Voltages when T_1 and T_2 are high.

The schematic used to test the NAND gate in Simulink® is shown in Figure 11. The truth table for the NAND gate is Table 3. The results for the simulation are shown in Figures 12 to 15.

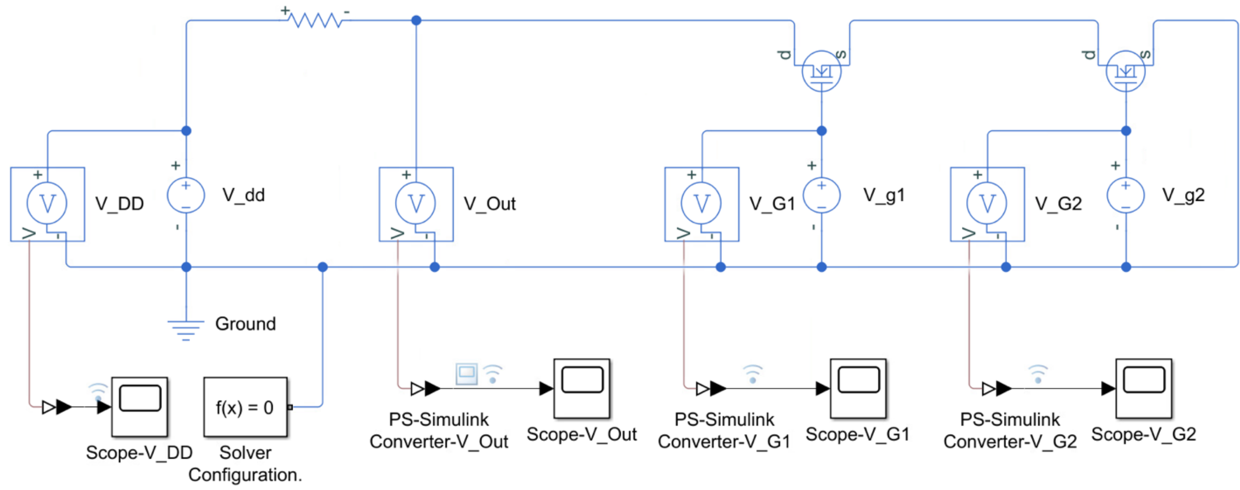


Figure 11: NAND Gate Circuit Simulation

Table 3: NAND Gate Truth Table

T_1	T_2	F
0	0	1
0	1	1
1	0	1
1	1	0

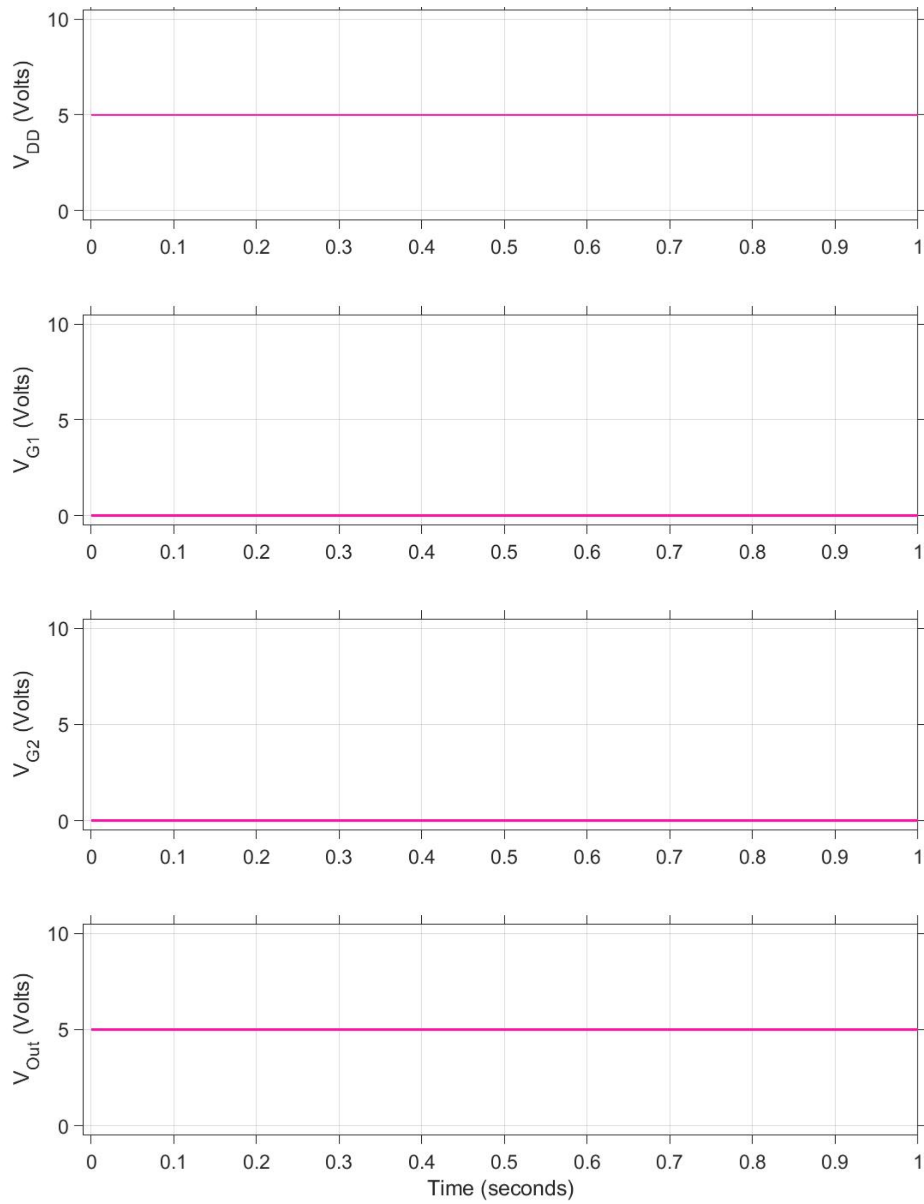


Figure 12: NAND Gate Circuit Voltages when T_1 and T_2 are low.

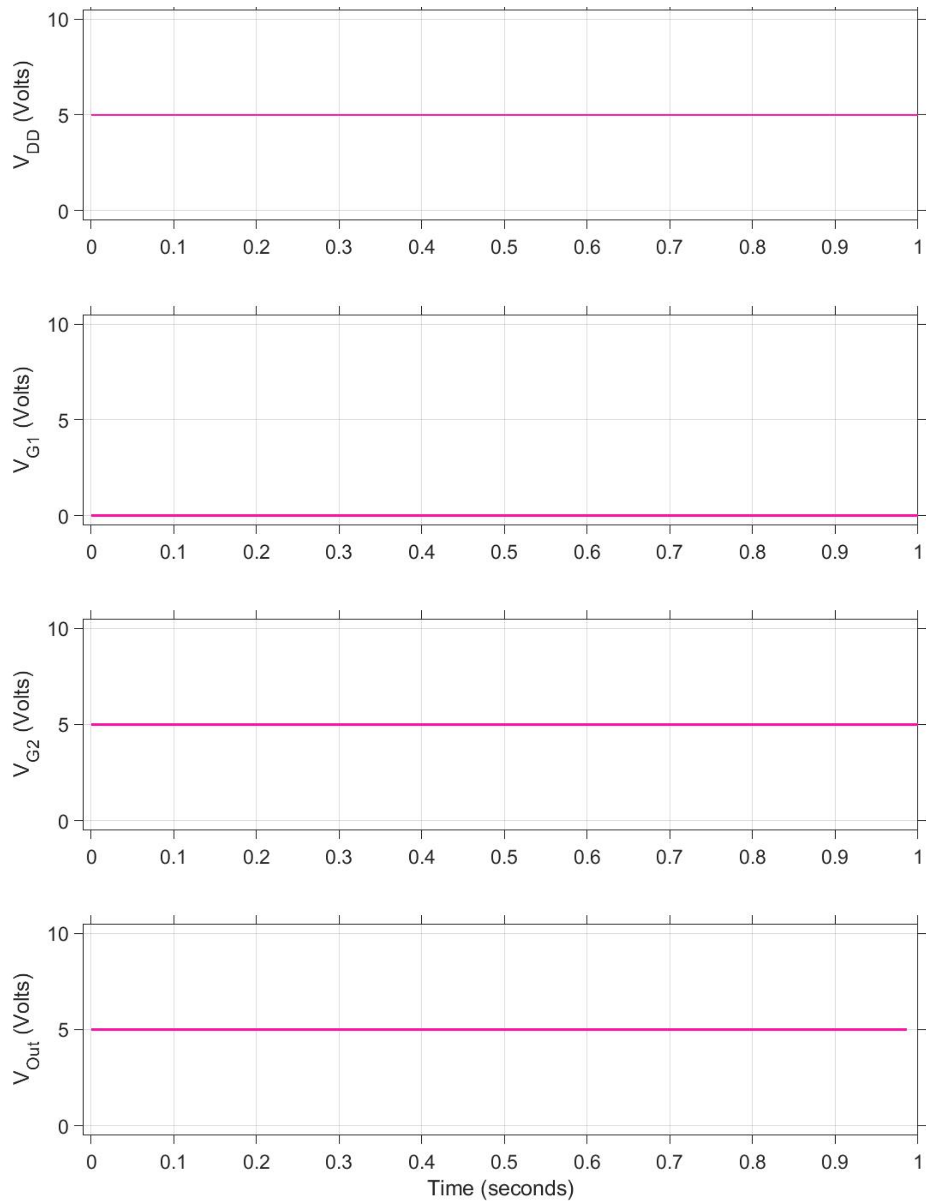


Figure 13: NAND Gate Circuit Voltages when T_1 is low and T_2 is high.

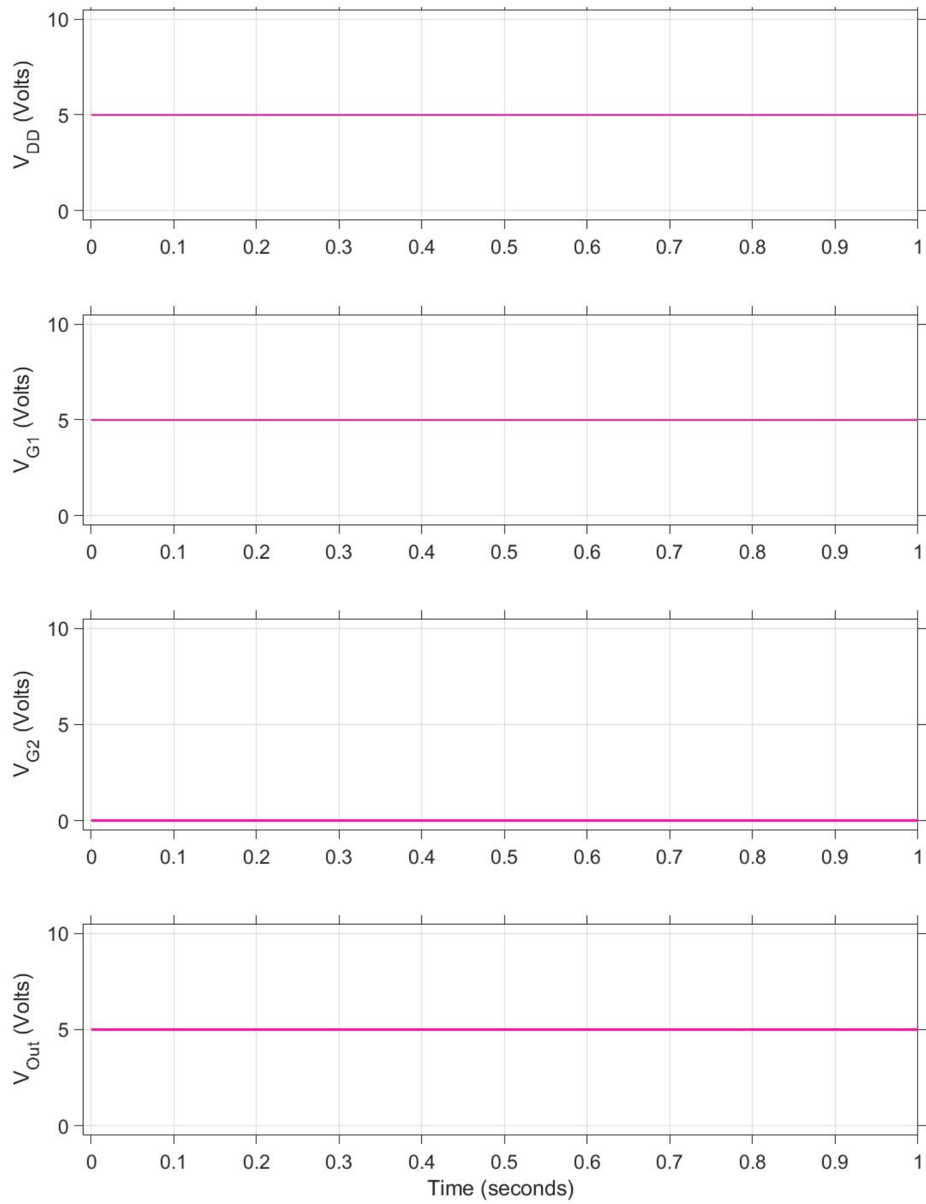


Figure 14: NAND Gate Circuit Voltages when T_1 is high and T_2 is low.

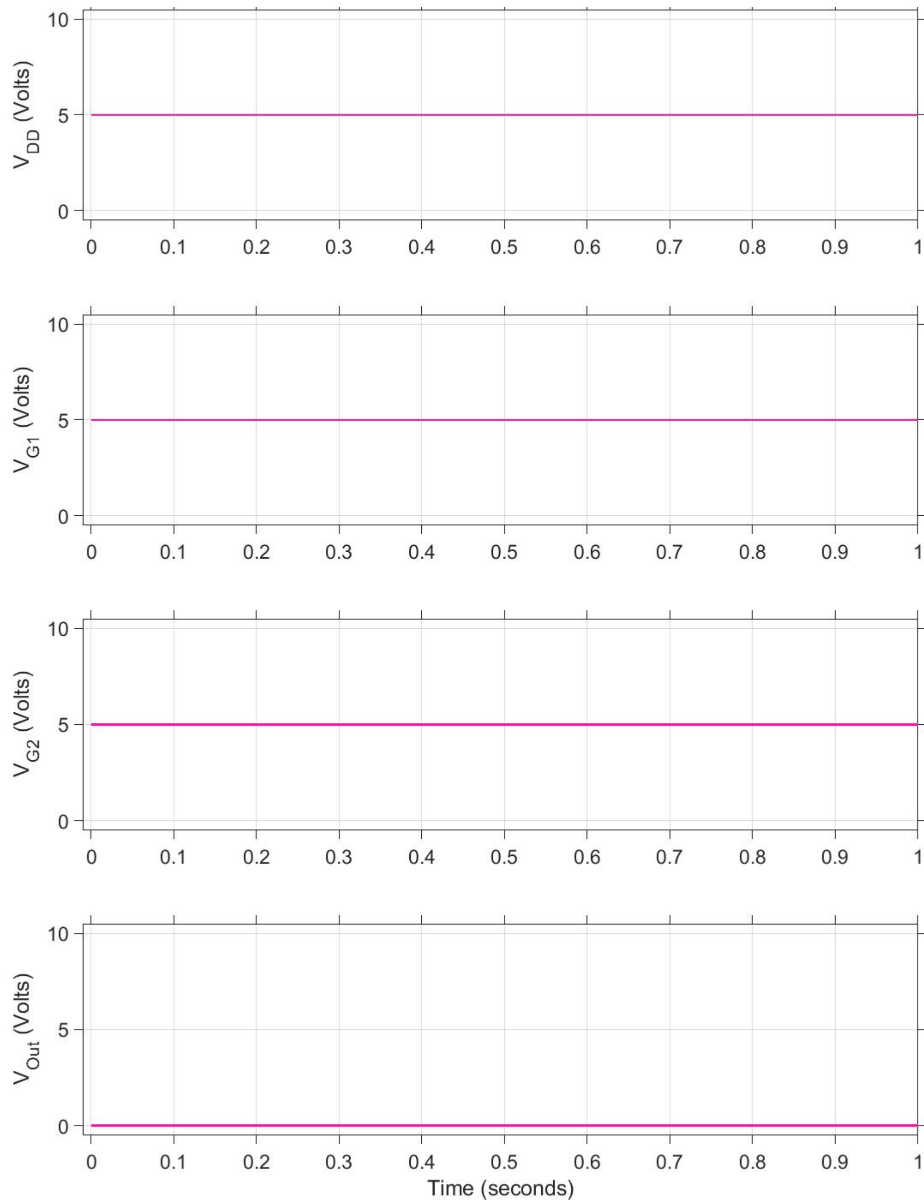


Figure 15: NAND Gate Circuit Voltages when T_1 and T_2 are high.

The schematic used to test the OR gate in Simulink® is shown in Figure 16. The OR gate is a composite gate made of the NOR gate and the NOT gate. The truth table for the OR gate is Table 4. The results for the simulation are shown in Figures 17 to 20.

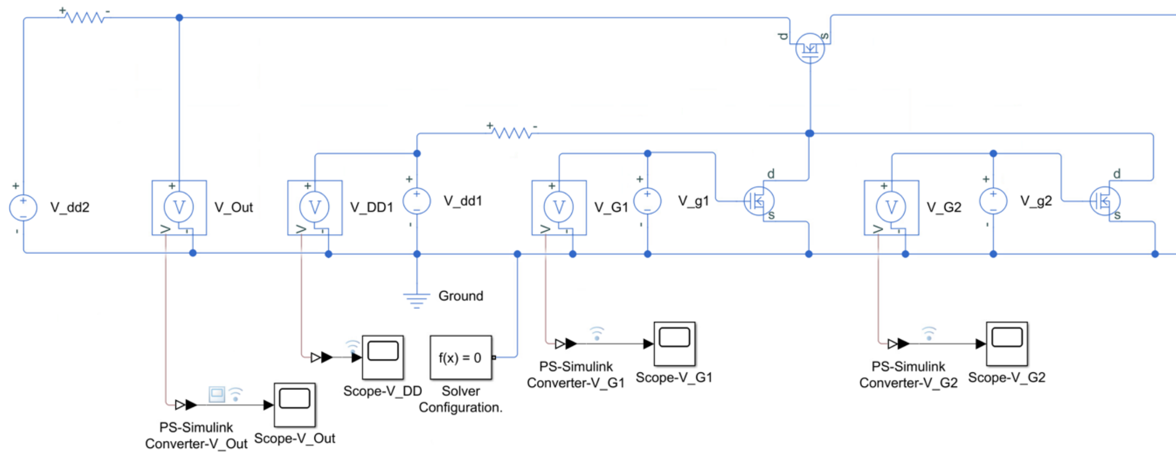


Figure 16: OR Gate Circuit Simulation

Table 4: OR Gate Truth Table

T_1	T_2	F
0	0	0
0	1	1
1	0	1
1	1	1

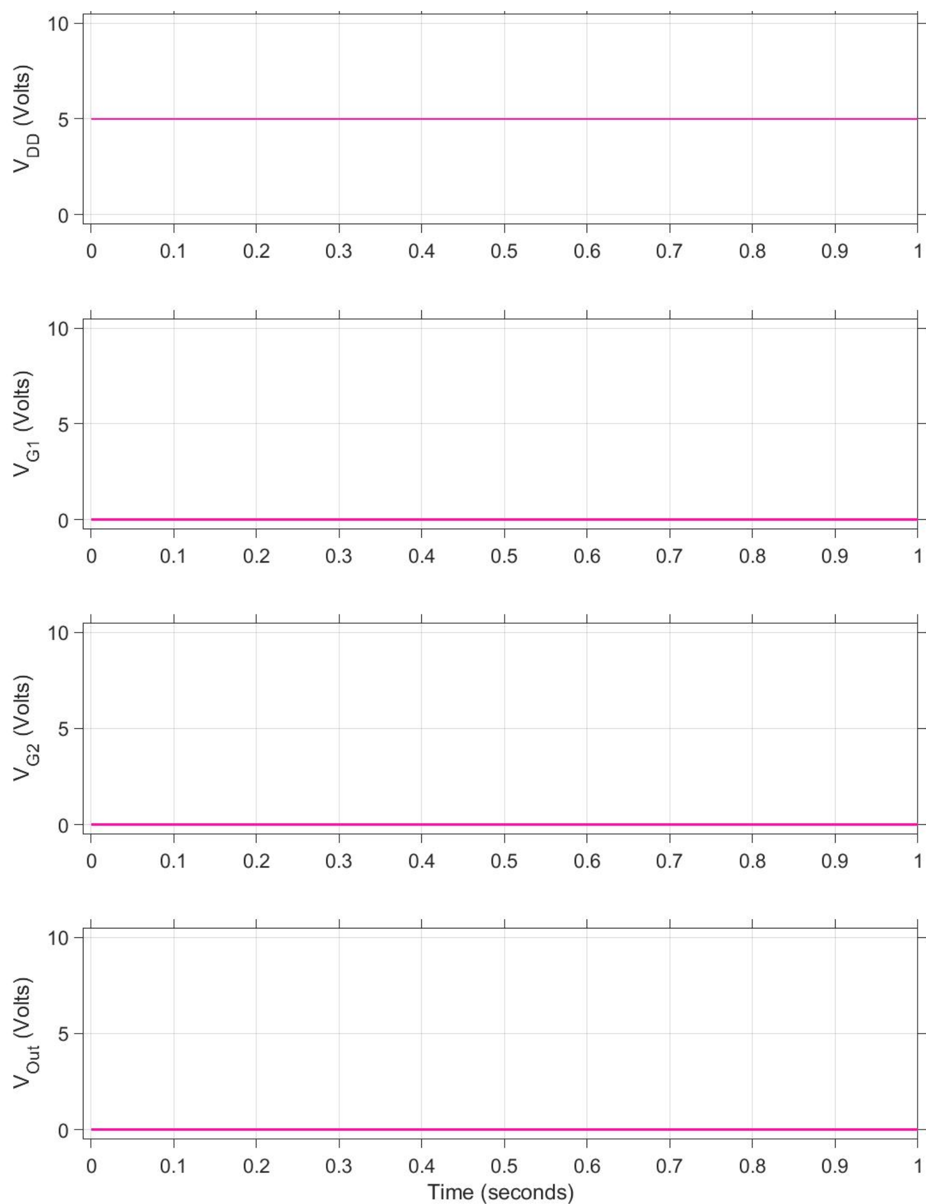


Figure 17: OR Gate Circuit Voltages when T_1 and T_2 are low.

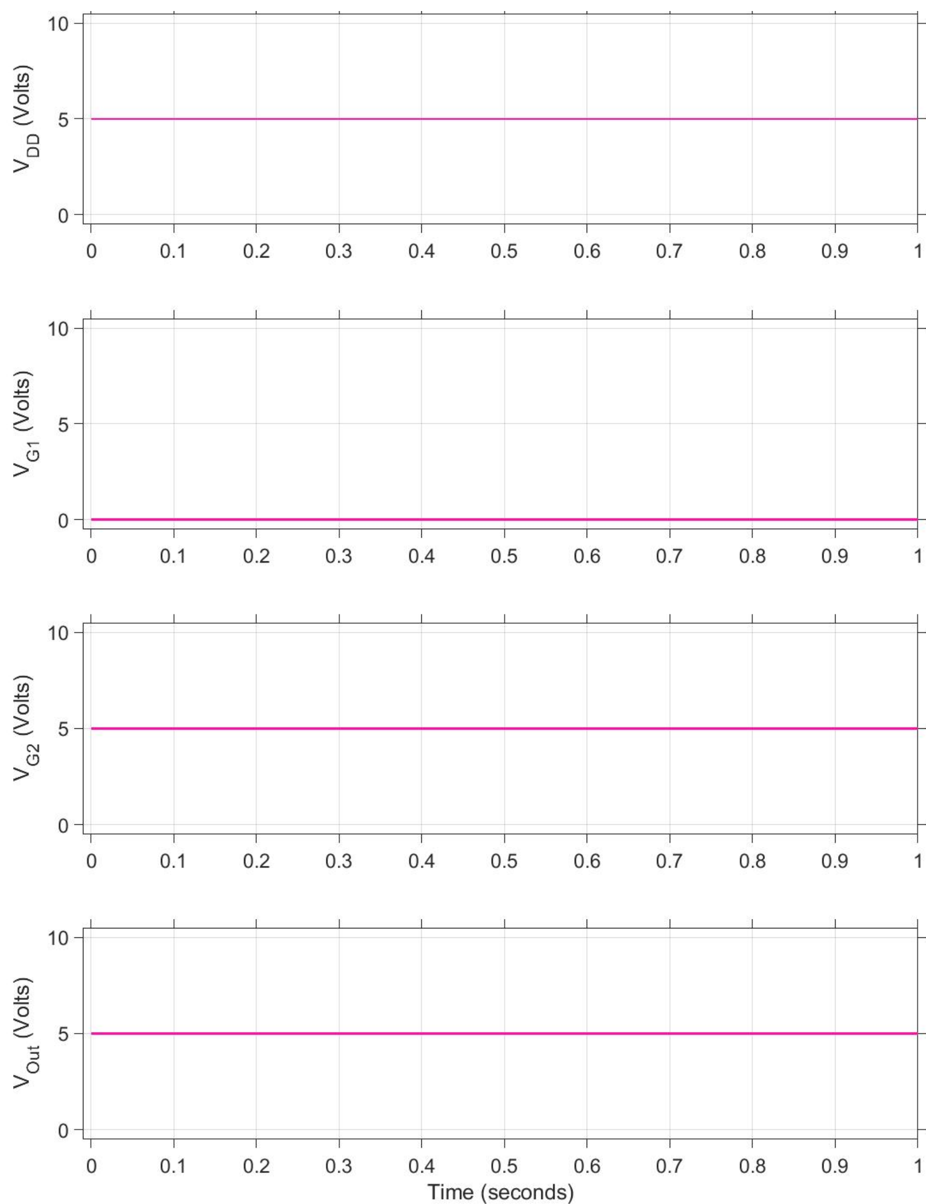


Figure 18: OR Gate Circuit Voltages when T_1 is low and T_2 is high.

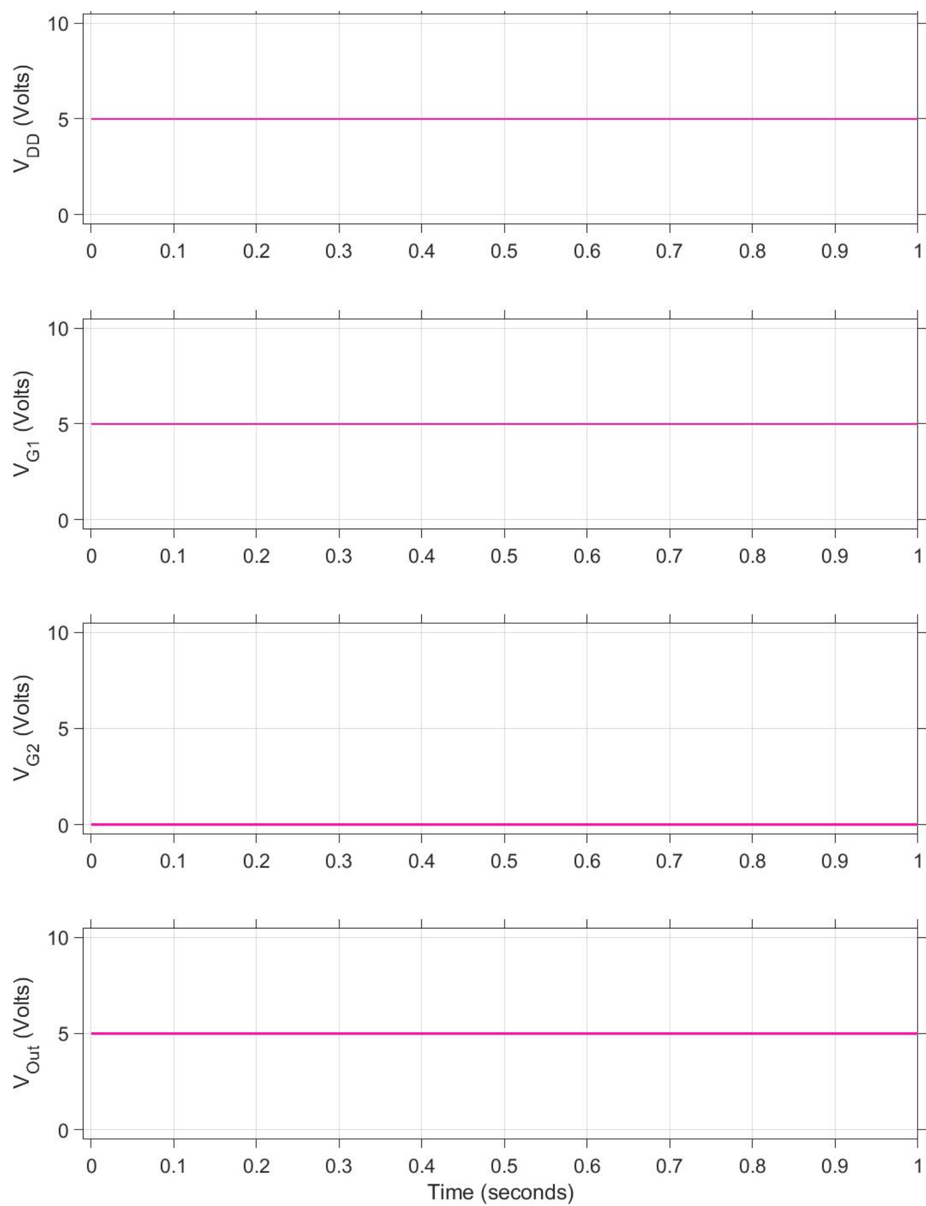


Figure 19: OR Gate Circuit Voltages when T_1 is high and T_2 is low.

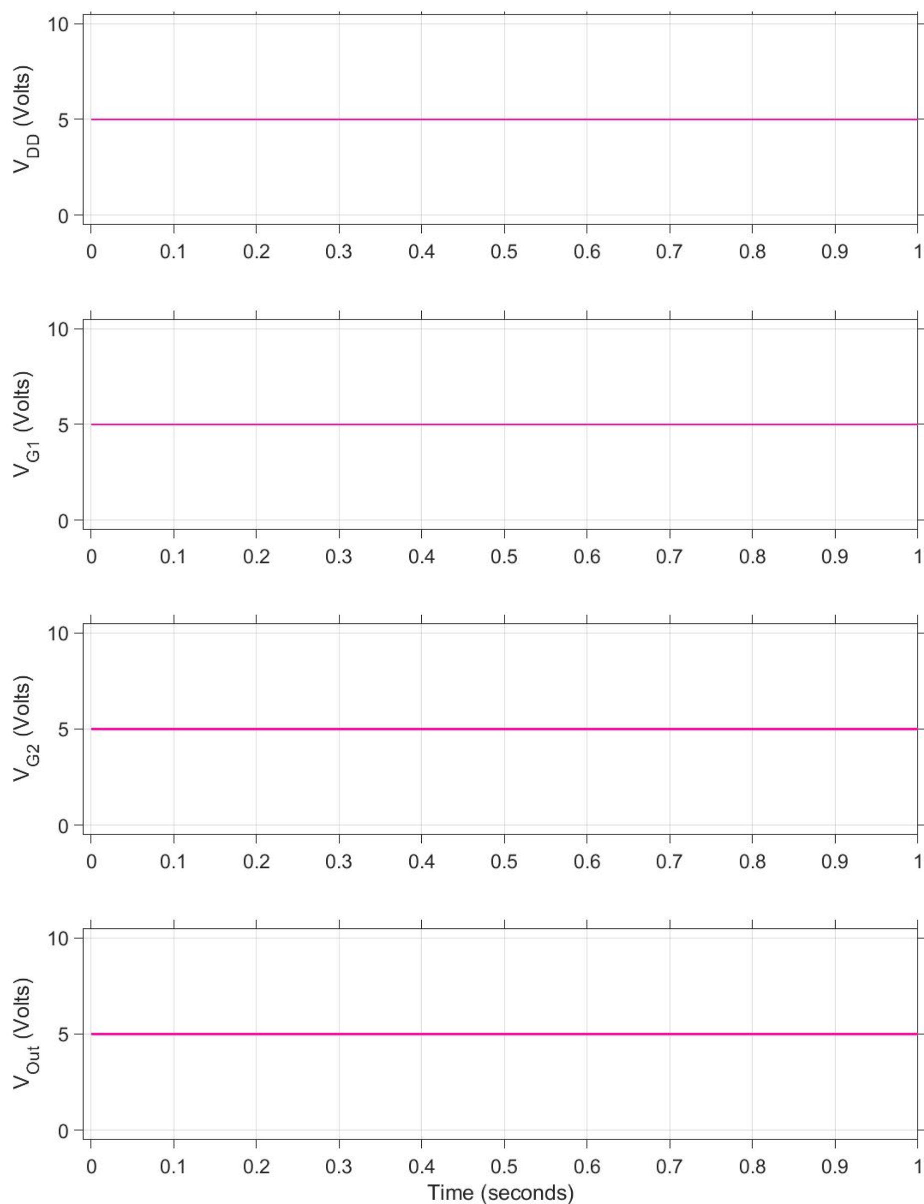


Figure 20: OR Gate Circuit Voltages when T_1 and T_2 are high.

The schematic used to test the AND gate in Simulink® is shown in Figure 21. The AND gate is a composite gate made of a NAND gate and a NOT gate. The truth table for the AND gate is Table 5. The results for the simulation are shown in Figures 22 to 25.

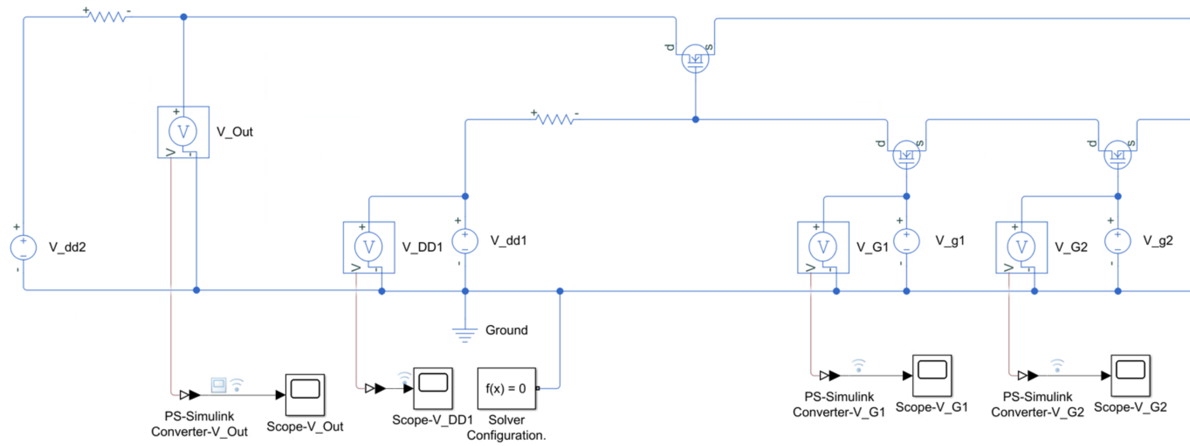


Figure 21: AND Gate Circuit Simulation

Table 5: AND Gate Truth Table

T_1	T_2	F
0	0	0
0	1	0
1	0	0
1	1	1

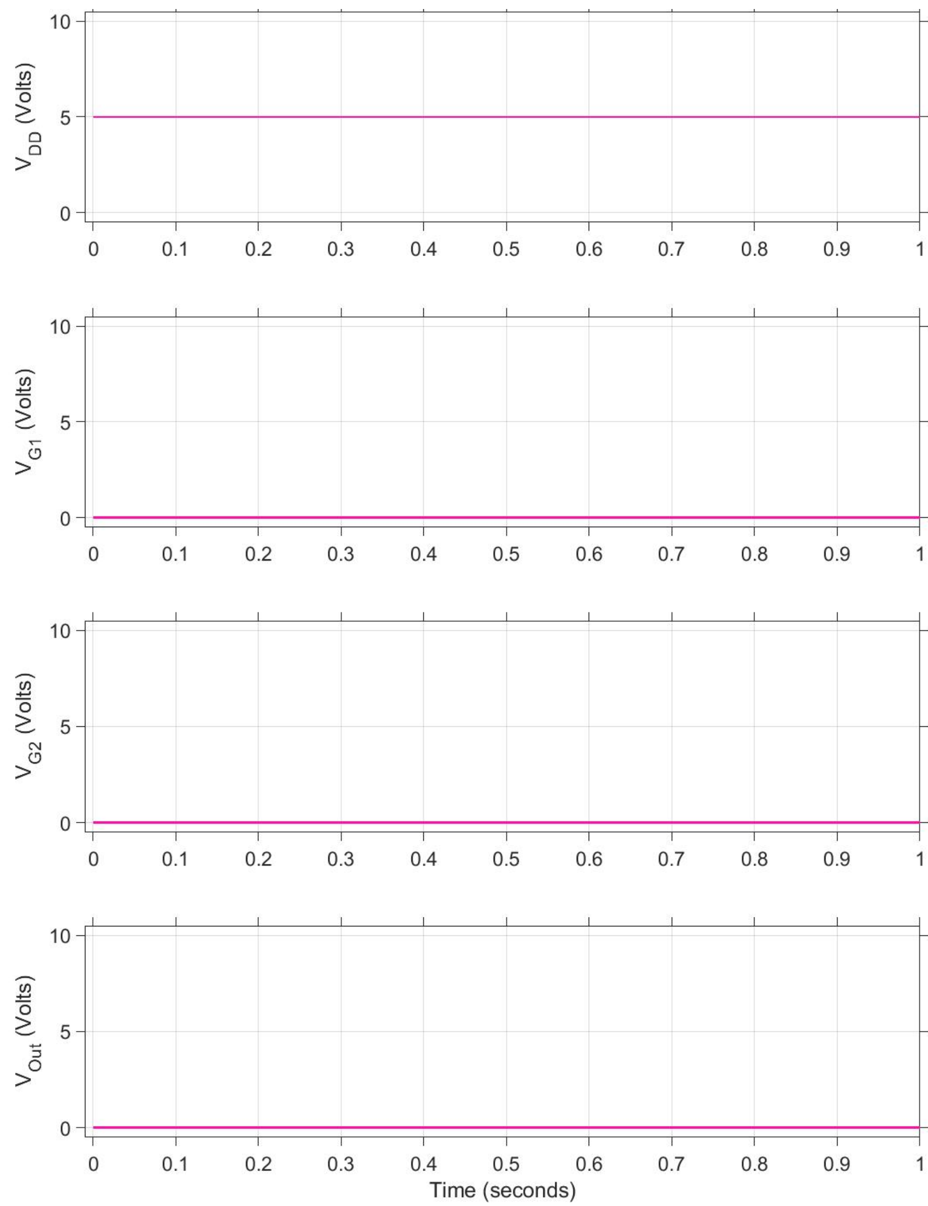


Figure 22: AND Gate Circuit Voltages when T_1 and T_2 are low.

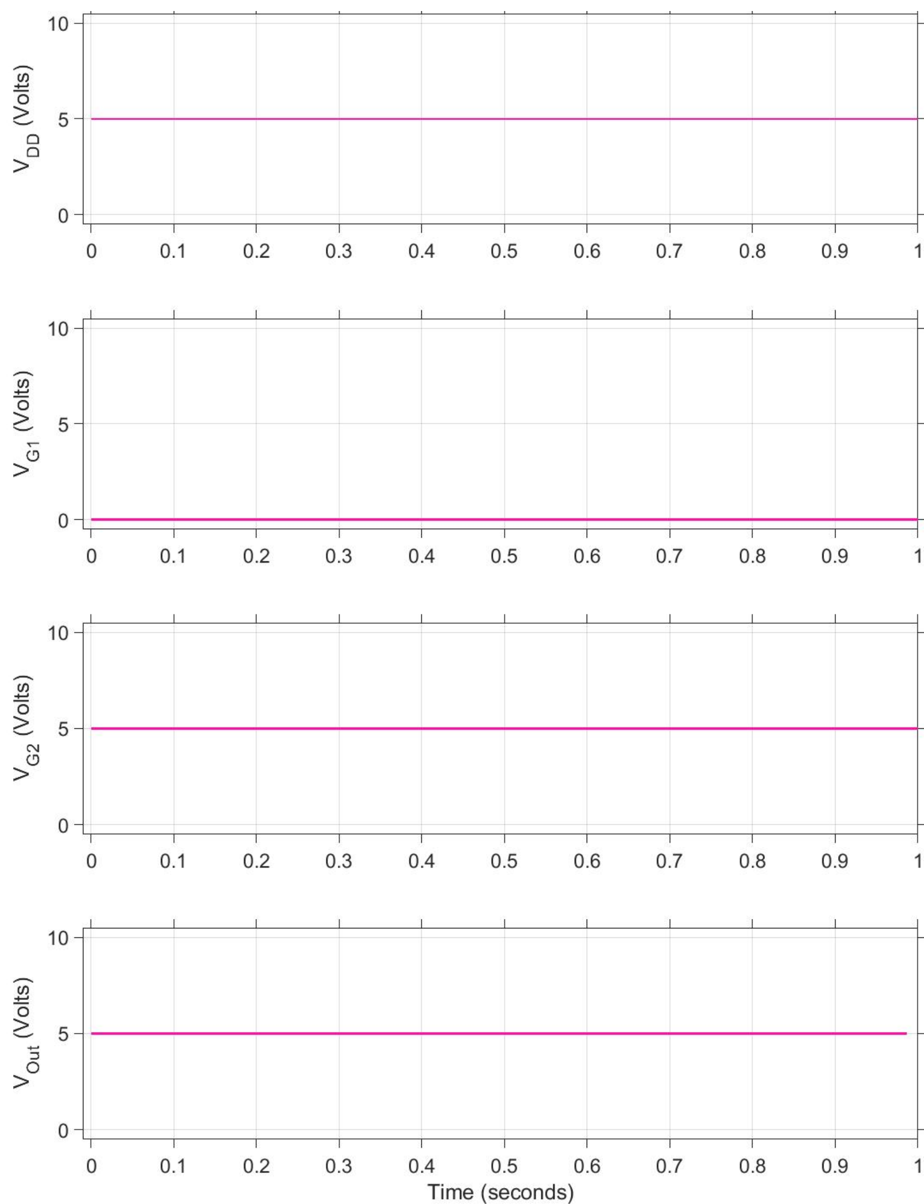


Figure 23: AND Gate Circuit Voltages when T_1 is low and T_2 is high.

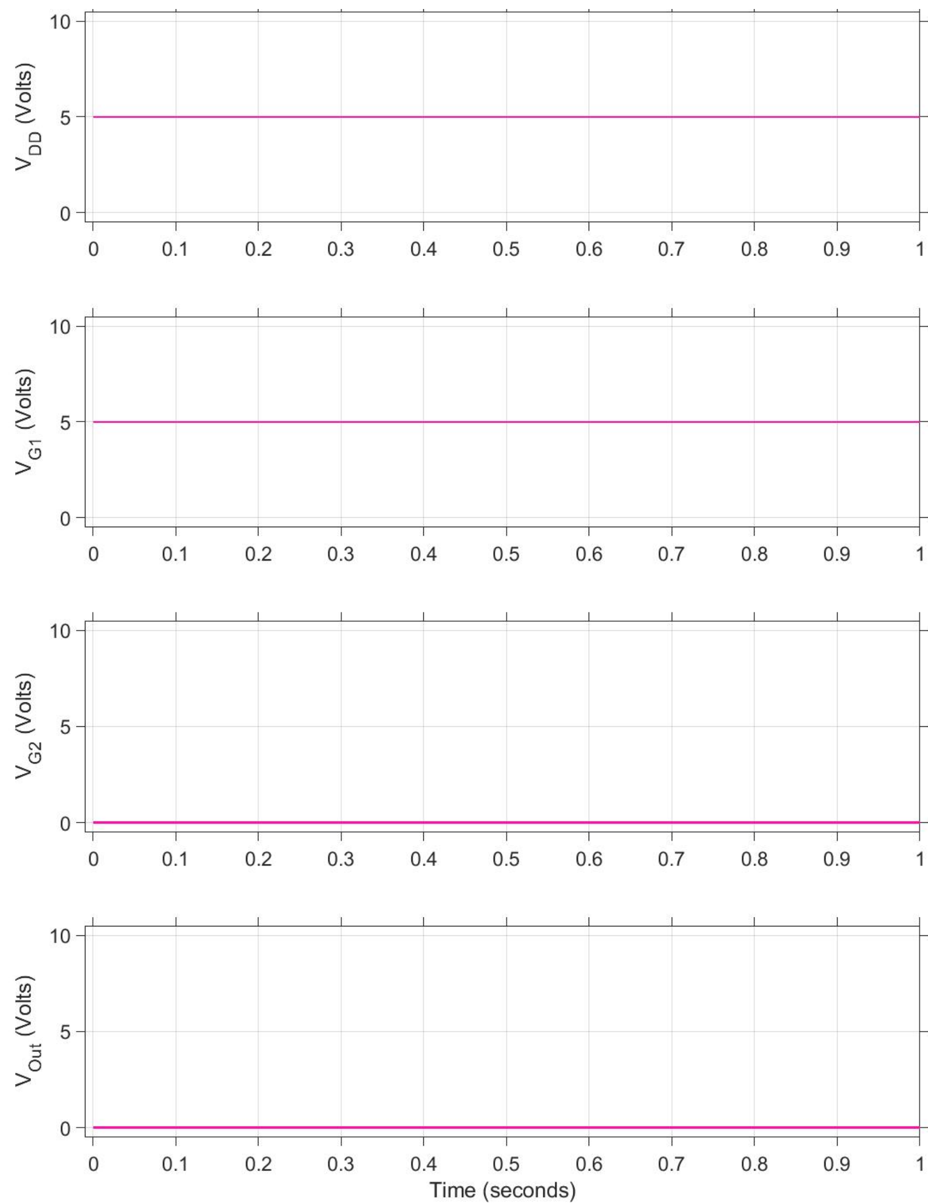


Figure 24: AND Gate Circuit Voltages when T_1 is high and T_2 is low.

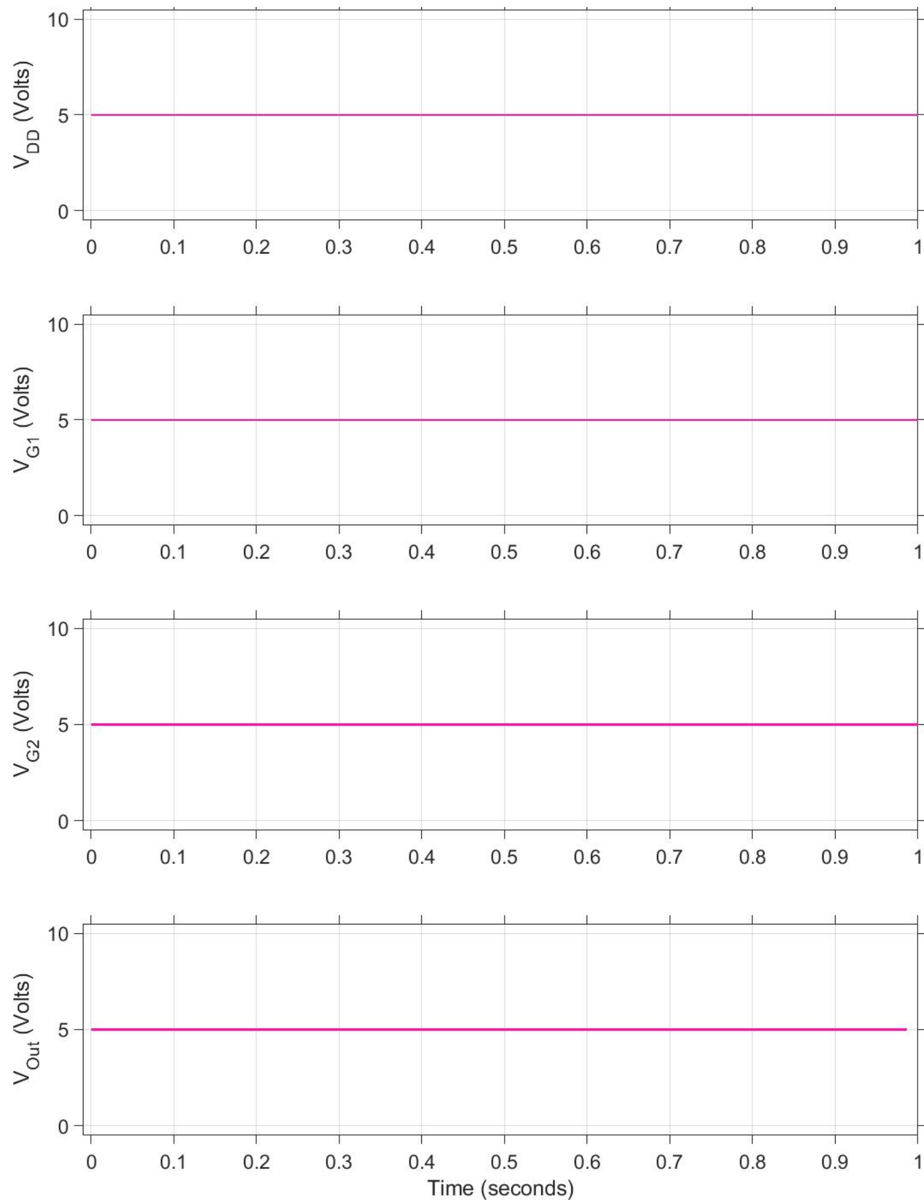


Figure 25: AND Gate Circuit Voltages when T_1 and T_2 are high.

2.2 Resistor Values

The resistor is another important component that needed to be considered when designing the circuit. One needs to know the amount of resistance that would stop the circuit from behaving properly. We used the NOR gate, with V_{DD} = 5 V, and the gate voltages either being 0 V or 5 V

depending on whether the signal needed to be low or high. The following values were tested: 100 kΩ, 10 kΩ, 1 kΩ, 100 Ω, 10 Ω, 1 Ω, and .1 Ω.

The only time the circuit stopped working was when the resistance was less than 1 Ω. A voltage output of 0 through 1 V is a logic 0. When either or both transistors were on, the voltage output was larger than the maximum acceptable value 1 V. When one transistor was on, then the output was 1.849 V. When both transistors were on, the output was 1.046 V. A resistor with less than 1 Ω is therefore the lowest value to be used in the circuit.

CHAPTER 3. FABRICATION

The silicon wafers were p-type (doped with boron) with a resistivity of 1 to 10 Ω-cm. The orientation was <100> and the diameter was 2 inches.

The first step in the fabrication process is to clean the wafer by removing organic contaminants and the natural oxide layer. The second step is to put the wafer in a furnace to grow the oxide layer that serves as the dielectric. The third step is the first of three photolithography processes. Photoresist (PR) is applied to the wafer, exposed to the diffusion window pattern, and developed. The fourth step is etching away part of the oxide layer to form the diffusion windows. The fifth step is stripping the photoresist off the wafer. The sixth step is pre-depositing the n-type dopant. The seventh step simultaneously grows the oxide layer while driving the dopant further into the wafer. The eighth step is the second of three photolithography processes. PR is applied to the wafer, exposed to the metal contact window pattern, and developed. The ninth step is etching away part of the oxide layer to form the metal contact windows. The tenth step is stripping the photoresist off the wafer. The eleventh step is using an electron beam to deposit aluminum over the entire wafer. The twelfth step is the last of three photolithography processes. PR is applied to the wafer, exposed to the metal contact pattern, and developed. The thirteenth step is etching away part of the metal layer to create separate metal contacts. The fourteenth step is stripping the photoresist off the wafer. The steps are illustrated in Figure 26. Each step will be detailed further in the upcoming section.

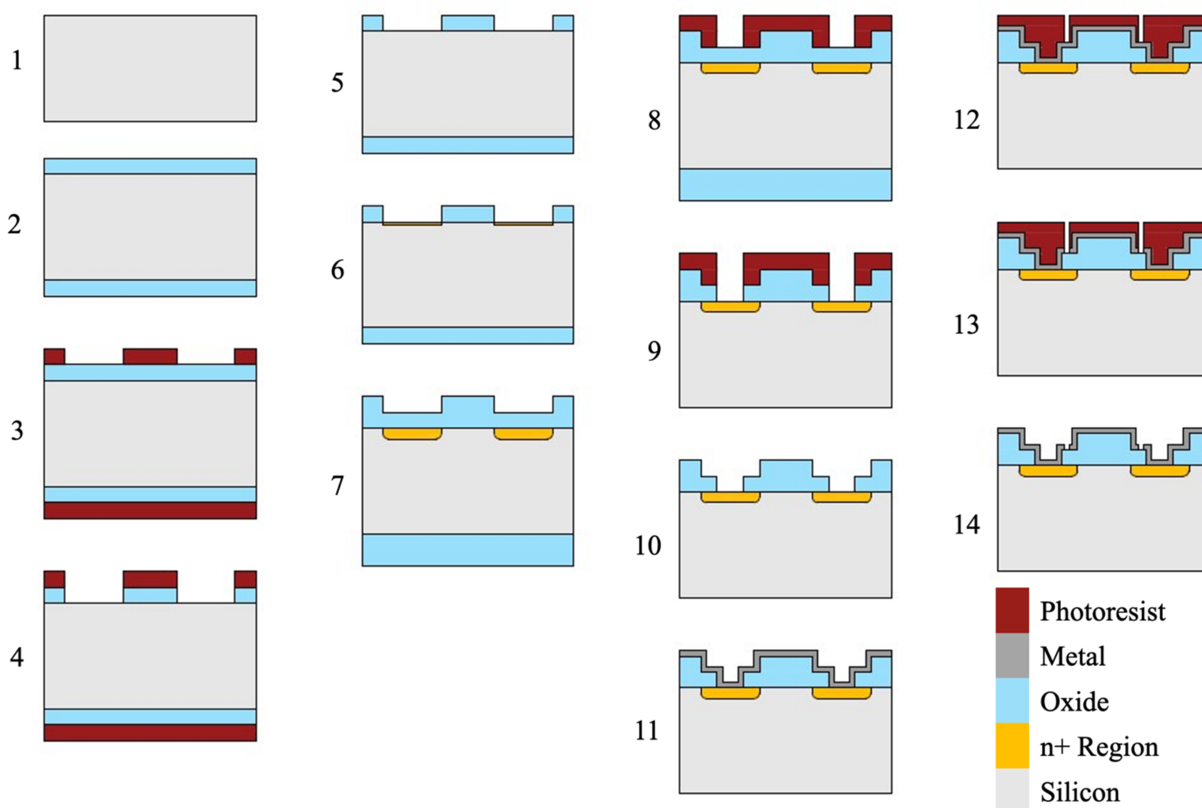


Figure 26: Step processes for the fabrication of the NMOS. Figure is not to scale.

3.1 Substrate Preparation

Organic contaminants must be removed from the wafer. A mixture of 50 parts sulfuric acid (H_2SO_4) and 1 part hydrogen peroxide (H_2O_2) are poured into a glass beaker. The beaker is then placed on a hot plate and the mixture is heated to 120°C. The heat will increase the solution's reactions with the organic particles on the wafer. The wafers are placed in a polytetrafluoroethylene (PTFE) wafer boat, and the wafer boat is placed into the mixture. The beaker is placed in an ultrasonic cleaner (Branson 5510) for 1 minute to loosen and remove particles off of the wafers. The beaker is removed from the ultrasonic cleaner. The wafers are individually rinsed with deionized (DI) water, dried with a nitrogen (N_2) gun, and placed into the

wafer boat. It is critical to use DI water instead of regular tap water to avoid pollution and unwanted contamination by ions present in regular tap water. Molecular nitrogen is an inert gas at room temperature, so it does not react with the wafer.

The natural oxide layer must also be removed from the wafer, because the quality and exact thickness is unknown. A PTFE beaker is filled with 2.5% hydrofluoric acid (HF). HF etches glass, but it does not react to PTFE, so HF is placed in a PTFE beaker instead of a glass beaker. The wafer boat is placed into the HF for 5 seconds. The wafers are individually rinsed with DI water and dried with a nitrogen gun.

3.2 Oxidation

In order to grow the dielectric material, the wafer is oxidized in a furnace. The oxidation process is done in a dry-wet-dry pattern. Dry oxidation occurs when oxygen is introduced in the furnace as a gas, and wet oxidation occurs when oxygen is introduced in the furnace in the form of water vapor. Dry oxidation is slower than wet oxidation, but the lower oxide growth rate allows the atoms to align better to create a higher quality interface between the silicon and the silicon dioxide (SiO_2). Wet oxidation is used for the middle portion of the oxide layer because the oxide quality is not as important in this area and the faster growth rate reduces the amount of time spent fabricating.

The wafers are transferred to a quartz wafer boat. Quartz is used because it does not melt at the temperatures used in the furnace and are chemically inert. A short, quartz push-rod pulls the wafer boat into a specific tube, called the elephant tube. The elephant tube is brought over to the furnace tube opening, the short push-rod pushes the wafer boat into the furnace tube opening, and the elephant tube and short push-rod are removed. Then, a long, quartz push-rod pushes the wafer

boat into the furnace in 1 minute. The wafer boat is slowly pushed in to prevent rapid and uneven thermal expansion in the wafers, which would cause them to crack. Changing the temperature of the wafer means changing the space between the atoms and having hot edges of the wafer that are trying to expand while the cooler middle area of the wafer is not expanding at a similar enough rate will cause the wafer to fracture. The long push-rod is placed back into its holder on top of the furnace. The furnace cap is then placed on the furnace tube opening. The oxidation furnace we used is the Lindberg Moldatherm Hinged Tube Furnace 55647. The oxidation furnace is circled in pink in Figure 27.

Figure 27: The oxidation furnace Lindberg Moldatherm Hinged Tube Furnace 55647.

Dry oxidation occurs for 10 minutes at a temperature of 1050°C, with O_2 pressure at 5 psi, and a flow rate of 1.2 lpm. Wet oxidation occurs for 13 minutes at a temperature of 1050°C, with N_2 pressure at 5 psi, and a flow rate of 0.3 lpm. Molecular nitrogen is still an inert gas at this temperature, so it is used because it will not react with the wafers. The nitrogen pushes the water into the furnace and prevents any other gas from entering. The hot plate beneath the beaker of water is set to 95°C. Dry oxidation occurs again for 12 minutes at a temperature of 1050°C, with O_2 pressure at 5 psi, and a flow rate of 1.2 lpm to ensure good interfaces on both sides.

When the oxidation process is finished, the furnace cap is removed, and the long push-rod pulls the wafer boat out of the furnace for 1 minute. The long push-rod is placed back into its holder on top of the furnace. The elephant tube is placed onto the open furnace tube, and the short push-rod pulls the wafer boat into the elephant tube. The elephant tube and short push-rod are removed from the furnace and placed on the counter to cool down for 10 minutes.

3.3 Photolithography for the Diffusion Window

Photolithography, also known as optical lithography, is the process that allows light to shine patterns onto photoresist and provides the framework for other processes to etch away or deposit material in order to permanently transfer the pattern onto the wafer. Photoresist (PR) is a material that reacts to light, and the areas of PR that are exposed to light will either become more or less soluble in the developer solution. When positive PR (+PR) is exposed to light, the +PR becomes more soluble in the developer solution [3]. When negative PR (-PR) is exposed to light, the -PR becomes less soluble in the developer solution [3]. -PR produces a pattern with lower resolution compared to +PR, because the -PR absorbs the developer and swells [3]. We used a +PR named AZ1512.

The purpose for the first photolithography step is to create a pattern where the oxide will later be etched away to establish windows of silicon, allowing the dopant to reach the semiconductor material and diffuse onto specific locations on the wafer. It is important to note that one cannot use the PR directly for patterning. The PR would deteriorate at the high temperatures of the furnace where the diffusion of the dopants occurs. Since the oxide does not change under the diffusion process conditions, the pattern is transferred to the oxide and then used

to form the pattern on the silicon. Thus, the oxide must be grown and then etched away to fully transfer the diffusion window pattern.

The PR must be applied to the wafer. The ambient or environmental lighting in the lab needs to be yellow, because the PR does not react to light with wavelengths greater than 0.5 μm [3]. The regular ceiling lights are turned off and the yellow lights are turned on. A spin coater is used to evenly distribute the +PR across the wafer. The wafer is placed on a spin coater chuck. The vacuum is turned on to hold the wafer to the chuck. An eye dropper is used to apply a thin layer of +PR to the wafer. Then, the spin coater lid is closed. The wafer spins at 500 rpm for 5 seconds to remove the excess PR and then 4500 rpm for 30 seconds to get the PR to the desired thickness. The spin coater is then opened, and the vacuum is released.

The wafer is taken to a small oven for a prebake. The prebake reduces the amount of solvent in the photoresist through evaporation in order to increase the PR's adhesion to the wafer and to stabilize the PR [9], [10]. The wafer is baked for 1 minute at 105°C.

Then, the oxide etch pattern must be transferred to the PR by exposing the PR to light. The wafer is placed into a mask aligner for exposure [11]. We used a μMLA Maskless Aligner by Heidelberg Instruments for our alignment and exposure system. Figure 28 is a photo of the μMLA Maskless Aligner by Heidelberg Instruments.

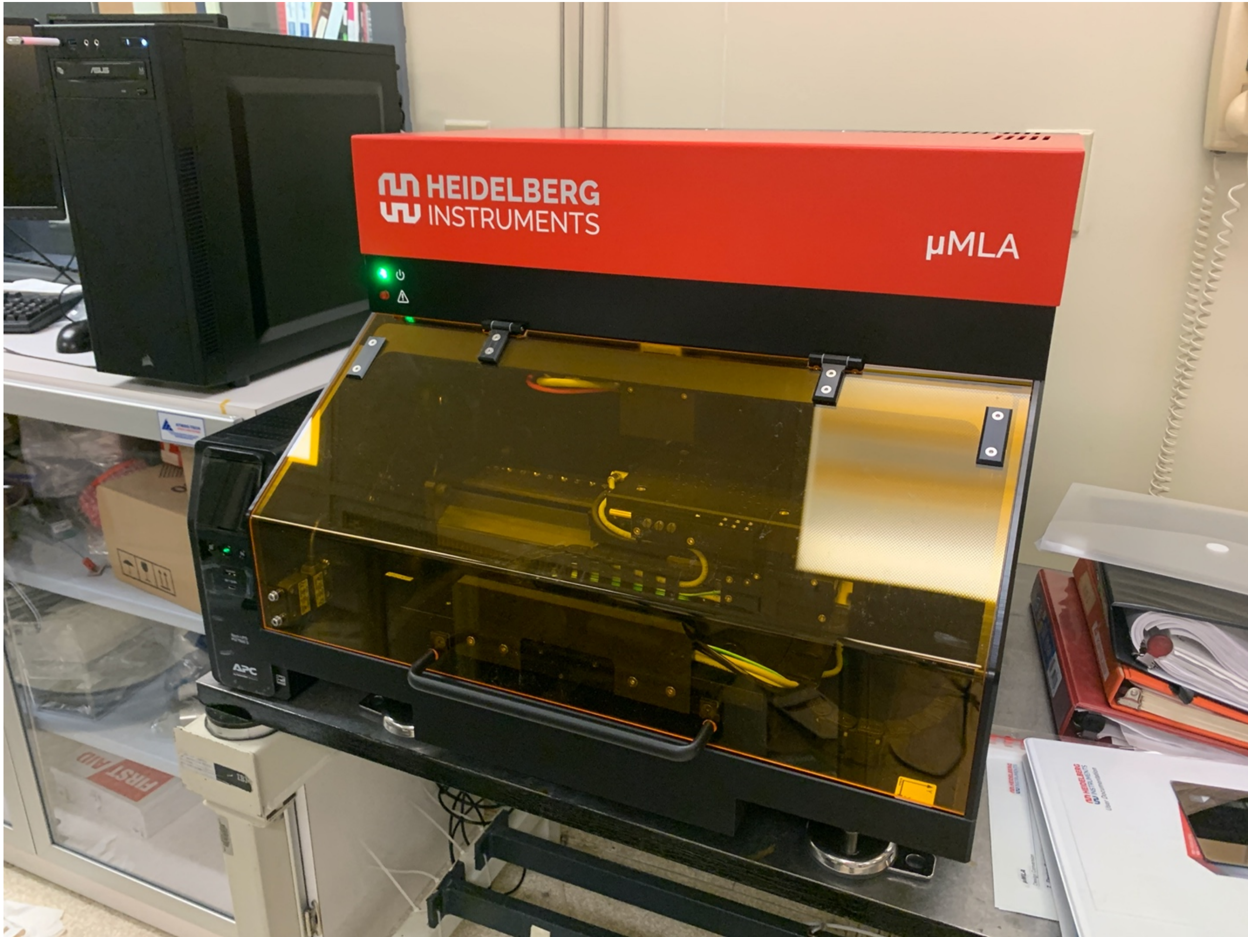


Figure 28: Photo of the µMLA Maskless Aligner by Heidelberg Instruments for the alignment and exposure system.

The wafer is taken to the oven for a post-exposure bake. The post-exposure bake helps to keep the pattern on the wafer while the developer is used. It also smooths out the edges of the pattern. During exposure, light is transmitted through the PR and reflected off of the shiny wafer surface beneath the PR [12]. This reflected light creates standing waves where areas in the exposed PR alternate between over and under exposure, which can thus be over and under developed [12]. The heat from baking allows the photosensitive compound in the PR to diffuse in order to allow the PR to be more evenly developed [9].

Then, the wafer is submerged into the developer (Az400k) for 40 seconds in order to remove the portions of the PR that were exposed to light. The wafer is rinsed in DI water and dried with a nitrogen gun.

Then, the wafer is taken to the oven for a post-bake. Similar to the prebake, the post-bake increases the adhesion of the PR to the wafer [3], [9].

3.4 Oxide Etch for Diffusion Window

The oxide layer must be etched in order to create windows for the silicon where the dopant will be diffused. The Buffer Oxide Etchant (BOE) is placed into a PTFE beaker. The BOE solution used is the Buffered oxide etch (5:1), CMOS™, J.T. Baker® and is primarily made of Ammonium Fluoride (NH_4F) and HF. PTFE tweezers are used to submerge the wafer into the BOE for 2 minutes. Then, the wafer is rinsed with DI water so that it may be handled with metal tweezers.

3.5 Strip Photoresist

The entire layer of photoresist must be removed. Acetone ($(CH_3)_2CO$) was used to strip the PR from the wafer. The wafer is held with metal tweezers as acetone is squirted onto the wafer. Then, the wafer was rinsed with DI water and dried with a nitrogen gun.

3.6 Pre-deposition

A dopant must be introduced in the substrate in order to form a p-n junction. The pre-deposition furnace is the Thermco mini-brute diffusion furnace (Model MB-80H). Figure 29 is a photo of the pre-deposition furnace. A separate furnace is used for pre-deposition in order to keep the oxidation furnace from being contaminated with dopants. The furnace is set to 950°C, the nitrogen pressure is 5 psi, and the flow rate is 1.2 lpm. The silicon wafers are placed in every other slot in the quartz pre-deposition wafer boat. The phosphorous diffusion wafers are Saint-Gobain PH-950. The diffusion wafers are placed in the slots in front of every silicon wafer.

Figure 29: The pre-deposition furnace is the Thermco mini-brute diffusion furnace (Model MB-80H).

Loading the wafer boat into the pre-deposition furnace follows the same procedure as loading the wafer boat into the oxidation furnace in Section 3.2. The dopant is pre-deposited onto the wafer for 30 minutes. When the pre-deposition process is finished, the wafer boat must be removed from the furnace. Unloading the wafer boat from the pre-deposition furnace is the same process as unloading the wafer boat from the oxidation furnace in Section 3.2.

3.7 Drive-In and Oxidation

The wafers must have the dopant driven further into the substrate and the oxide layer must be grown. Oxidation must occur again so that the gate oxide and the metal contact for the gate may reach beyond the edges of the doped regions in order to ensure that there is an even electric field applied between the source and drain. Figure 30 shows how the different gate oxide and metal contact lengths would affect the electric field between the doped regions. The silicon wafers are moved to the quartz oxidation wafer boat. Loading the wafer boat into the furnace follows the same procedure as the first oxidation process in Section 3.2.

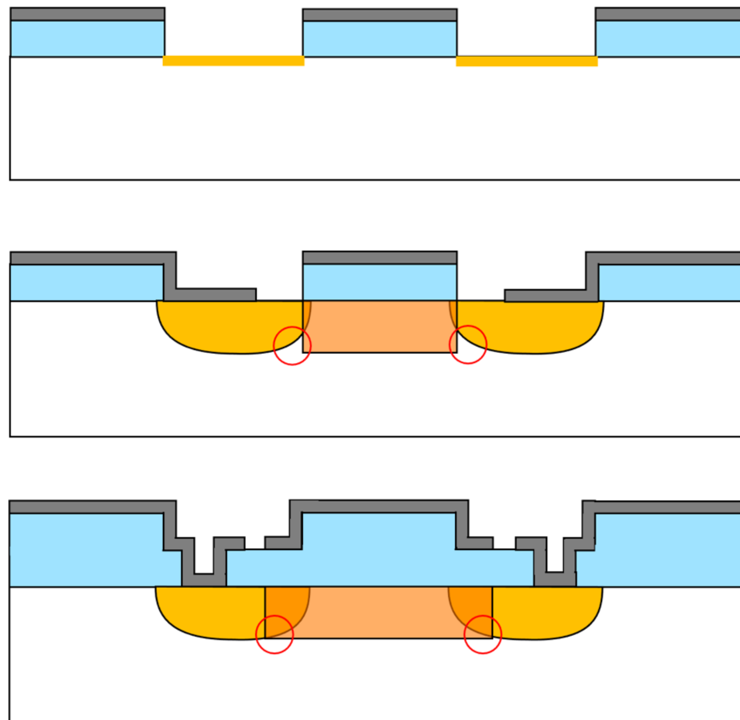


Figure 30: Schematic showing the effect of gate oxide on the electric field. The orange region represents the electric field, the yellow regions represent the doped regions, the blue regions represent the dielectric, and the gray regions represent the metal regions. The areas within the red circles note areas of interest.

Dry oxidation occurs for 10 minutes at a temperature of 1050°C, with O_2 pressure at 5 psi, and a flow rate of 1.2 lpm. Wet oxidation occurs for 5 minutes at a temperature of 1050°C, with N_2 pressure at 5 psi, and a flow rate of .3 lpm. The hot plate beneath the beaker of water is set to 95°C. Dry oxidation occurs again for 12 minutes at a temperature of 1050°C, with O_2 pressure at 5 psi, and a flow rate of 1.2 lpm.

When the oxidation process is finished, unloading the wafer boat from the oxidation furnace follows the same procedure as the first oxidation process in Section 3.2.

3.8 Photolithography for Metal Contact Windows

This is the second of the three photolithography processes. The purpose for this photolithography step is to create a pattern where the oxide will later be etched away to establish metal contact windows where the doped Si will touch the metal. The photolithography procedure follows the same procedure as in Section 3.3.

3.9 Oxide Etch for Metal Contact Windows

The oxide layer must be etched in order to create metal contact windows. The oxide etch procedure follows the same procedure as in Section 3.4.

3.10 Strip Photoresist

The procedure to remove the PR follows the same procedure identified in Section 3.5.

3.11 Metallization

Metal must be deposited to create a metal-semiconductor interface that will allow electrons to move from the doped regions and into the metal and around a desired path in the circuit. An electron beam (e-beam) (KJL PVD 75) is used to deposit aluminum (Al) onto the wafers. Figure

31 shows the e-beam system used. Aluminum is used because it is cheap, has very low resistance, and makes a good contact with SiO_2.

Figure 31: The electron beam that deposits aluminum is a KJL PVD 75.

The wafers are loaded into the substrate holder and placed into the evaporator chamber. Aluminum pellets are placed inside a crucible, and then the crucible is placed into the evaporator chamber. A vacuum must then be established. A vacuum is necessary because the metal in the crucible would react to the air, and the air molecules would block the Al atoms' paths to the wafer and reduce the rate of deposition. The mechanical pump was turned on to bring the pressure down from 800 torr to 0.1 torr. Then, the turbo pump brings the pressure down from 0.1 torr to 4.6×10^{-5} torr. Once the vacuum is established, the substrate holder is set to rotate in order to prevent an uneven distribution of metal in the wafers' windows. Then, the e-beam shutter was opened in order to uncover the crystal sensor that lets the computer calculate the rate of deposition. Power was applied to the tungsten (W) filament. The voltage was 8 kV and the current through the filament was slowly ramped up at a rate of 1 mA for every 15 s until the current reached 30 mA. The ramp up rate is slow in order to prevent the Al from spilling out of the crucible. The current heats up the filament and thermionic emission allows electrons to be emitted from the filament. A magnetic field controls the path of the electrons so they bombard the Al in the crucible. The Al heats up and evaporates. Al is deposited until there is a film thickness of 300 nm. Once the desired amount of Al has been deposited, the substrate and e-beam shutters are closed, slowly ramped down the current to 0 mA at a rate of 1 mA for every 15 s, turned off the power supply to the e-beam, turned the substrate rotation off, then vented the chamber to get it back to atmospheric pressure.

3.12 Photolithography for Metal Contacts

This is the third of the three photolithography processes. The purpose for this photolithography step is to create a pattern to etch away the metal in order to create individual metal contacts. The photolithography procedure follows the same procedure as in Section 3.3.

3.13 Metal Etch

The Al must be etched away in order to create individual metal contacts. The etchant solution is made of 380 mL phosphoric acid (H_3PO_4), 75 mL acetic acid (CH_3COOH), 25 mL DI water, and 15 mL nitric acid (HNO_3). The etchant solution is placed into a glass beaker. Since the etchant solution reacts with metal, the wafers are handled with PTFE tweezers. The wafers are submerged in the etchant solution for 5 minutes. Then, they are briefly submerged in DI water, so the wafers can be safely handled with metal tweezers.

3.14 Strip Photoresist

The procedure to remove the PR follows the same procedure identified in Section 3.5. The MOSFET is finished and is now ready to be characterized.

CHAPTER 4. GATE DESIGN AND CHARACTERIZATION RESULTS

4.1 Gate Layout Designs

The program we used to design the layouts of the gates was KLayout. In all of these layouts, the red layer represents the dopant diffusion windows, the violet layer represents the metal contact windows, and the blue violet layer represents the metal contacts. The red and violet shapes represent the areas that are exposed, developed, and etched away. In the blue violet layer, any area that is not blue violet is exposed, developed, and etched away. Isolated transistors and resistors have also been drawn.

The NOT gate, also known as an inverter, is the simplest gate, so the NOT gate was designed first. Unsure about which gate length and which resistor we should use, we created different combinations of gate lengths and resistors. Figure 32 shows the layout featuring various transistor and resistor combinations. The channel lengths consisted of 200 µm, 150 µm, 100 µm, and 75 µm. There were three different resistors. The length of the medium resistor was half the length of the largest resistor, and the length of the smallest resistor was a quarter of the length of the largest resistor. Figure 33 shows a close-up of an inverter with a gate length of 200 µm paired with the largest resistor. The design also includes isolated devices at the top of the layout, so the individual characteristics could be checked (see Figure 32).

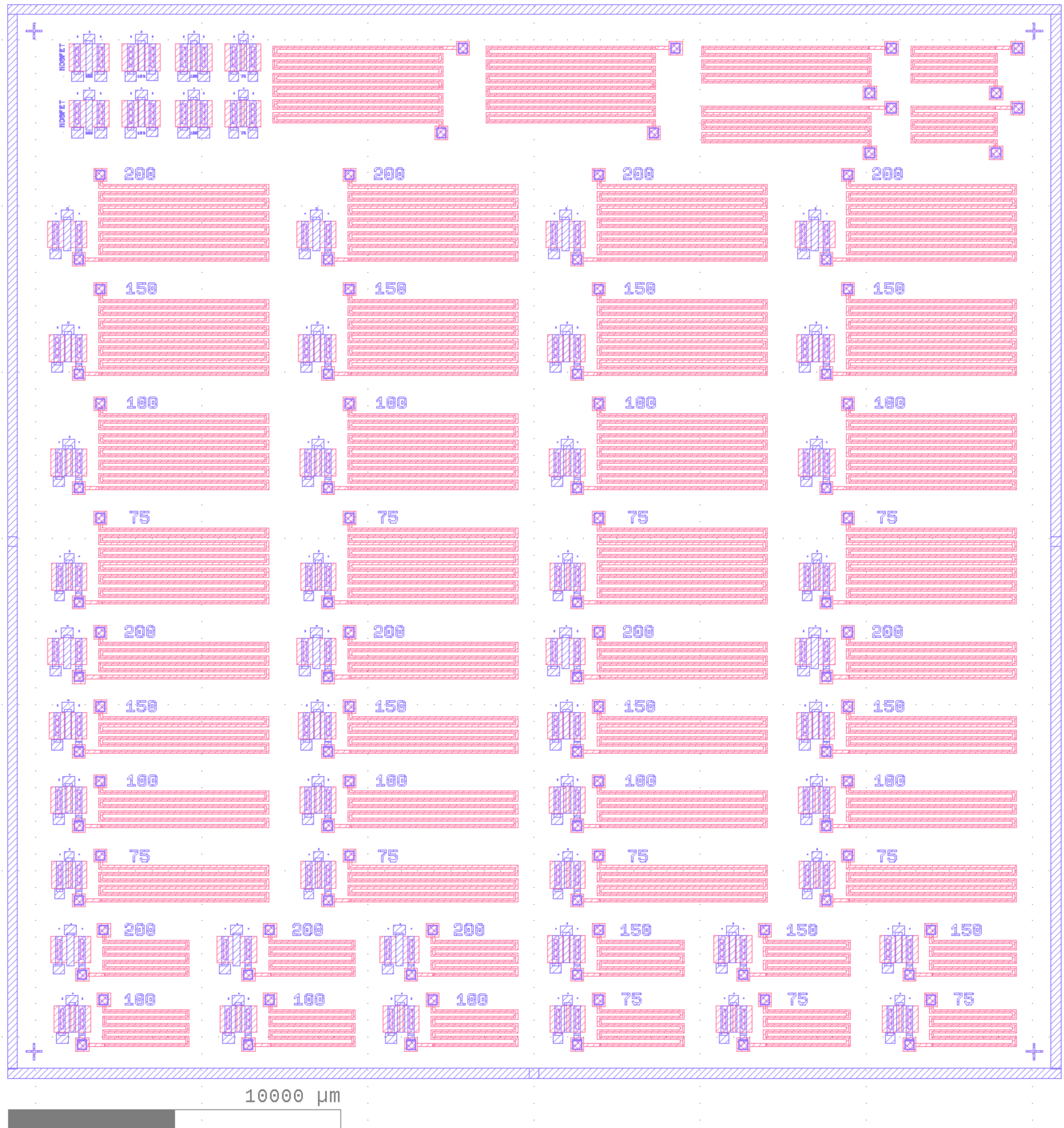


Figure 32: KLayout design featuring various transistor channel lengths (200 µm, 150 µm, 100 µm, and 75 µm) and resistor combinations.

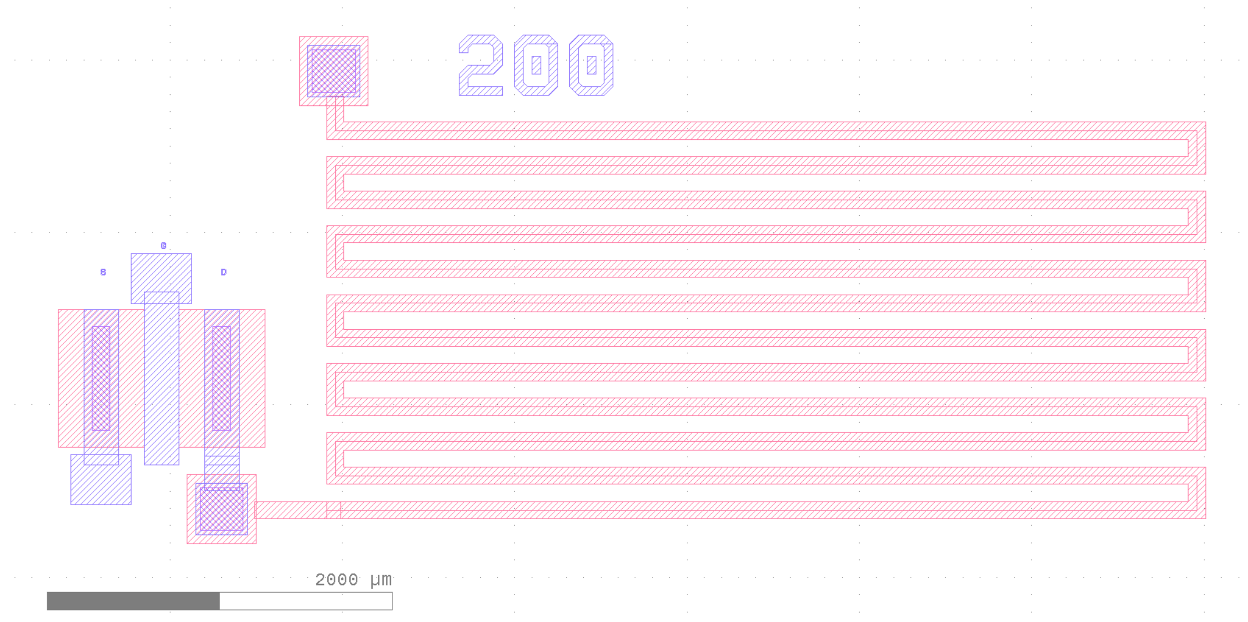


Figure 33: Close up of inverter with gate length of 200 µm paired with the largest resistor.

Then, a layout was designed so that a wafer would contain all the logic gates. Figure 34 shows the layout featuring NOT, NOR, NAND, OR, and AND gates. There were not enough probe holders and voltage supplies available in the lab in order to independently supply a voltage source V_{DD}, two gate voltages, and provide a ground, so the NOR, NAND, OR, and AND gates were each designed to have both inputs permanently connected to ground, one input permanently connected to a metal contact with a value of V_{GS} while the other input was permanently connected to ground, and both inputs permanently connected to the metal contact with a value of V_{GS}. Due to the redundancy of having a design where input A is HIGH and input B is LOW would give the same results as another design where input A is LOW and input B is HIGH, the gates would only have one design when one input is HIGH and the other input is LOW instead of having two separate designs. Figures 35 to 38 show close up views of NOR, NAND, OR, and AND gates with the metal contacts labelled. Each logic gate has transistors with a channel length of 75 µm and has the

largest resistor from the NOT gate wafer. The choice for channel length and resistor will be discussed in the next section. The metal contacts were also made to be larger in order to accommodate the task of placing the probes without the ability to finely adjust the probes' placement.

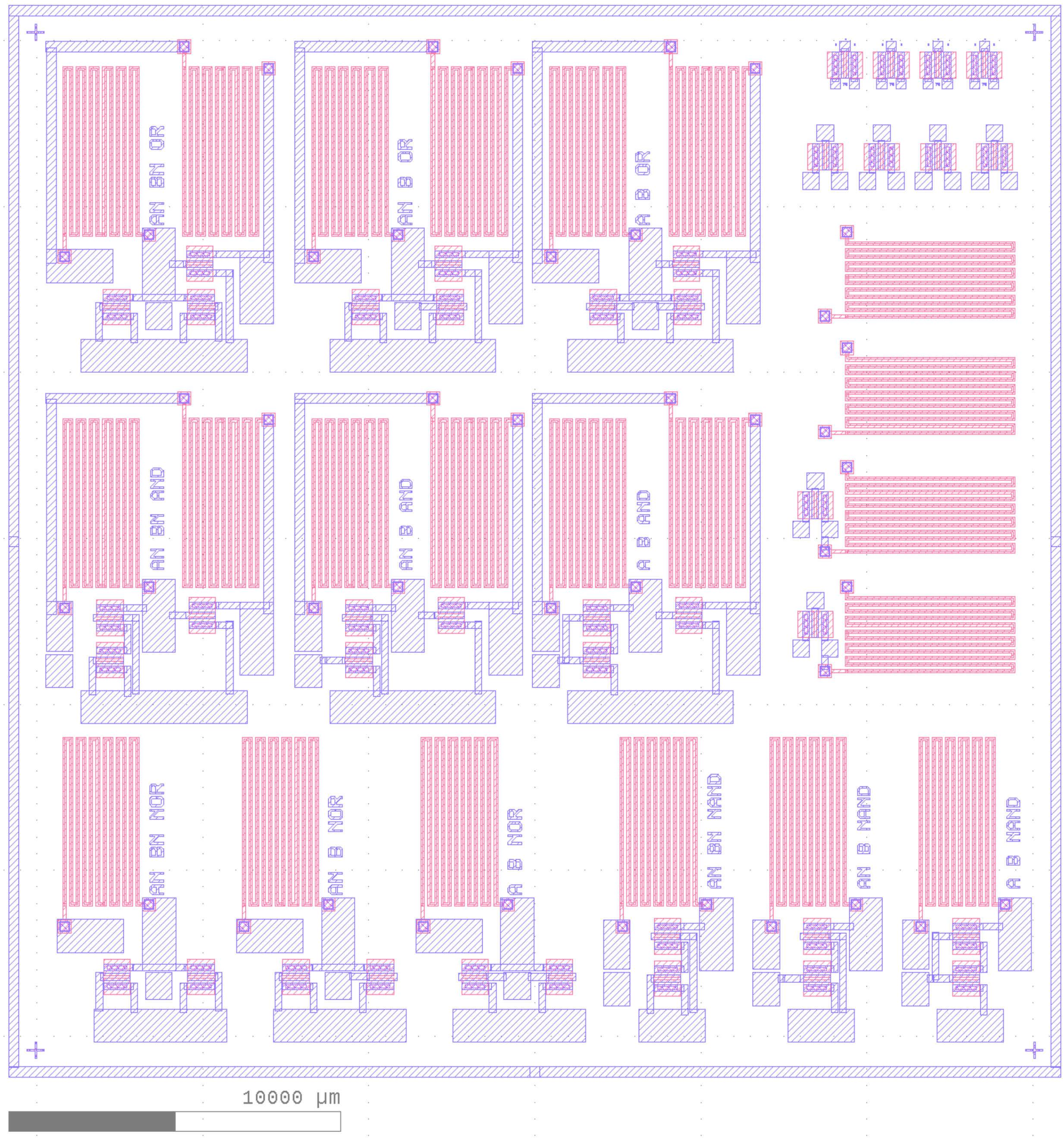


Figure 34: KLayout design featuring NOT, NOR, NAND, OR, and AND gates.

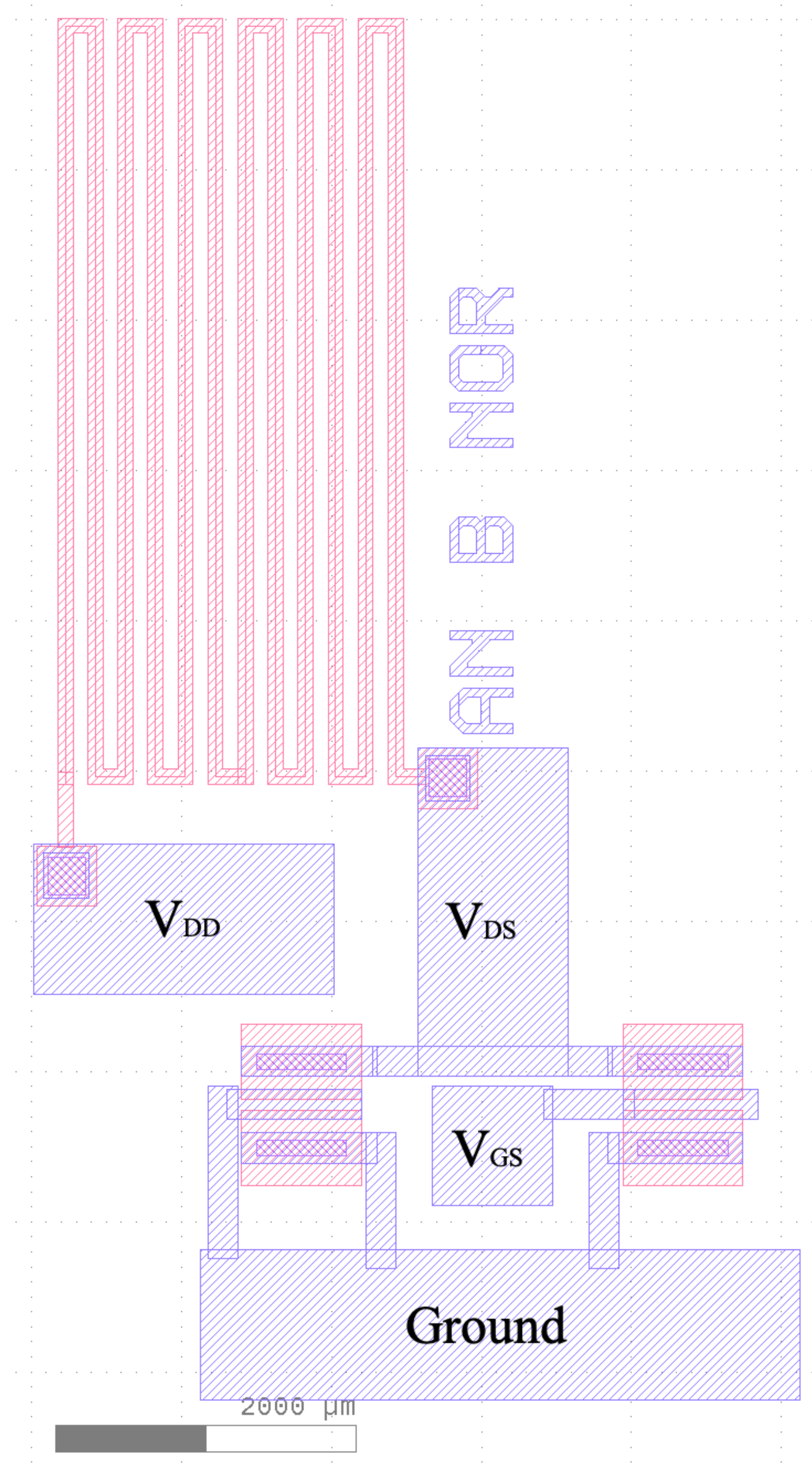


Figure 35: Close-up of the layout featuring the NOR gate with channel length of 75 µm.

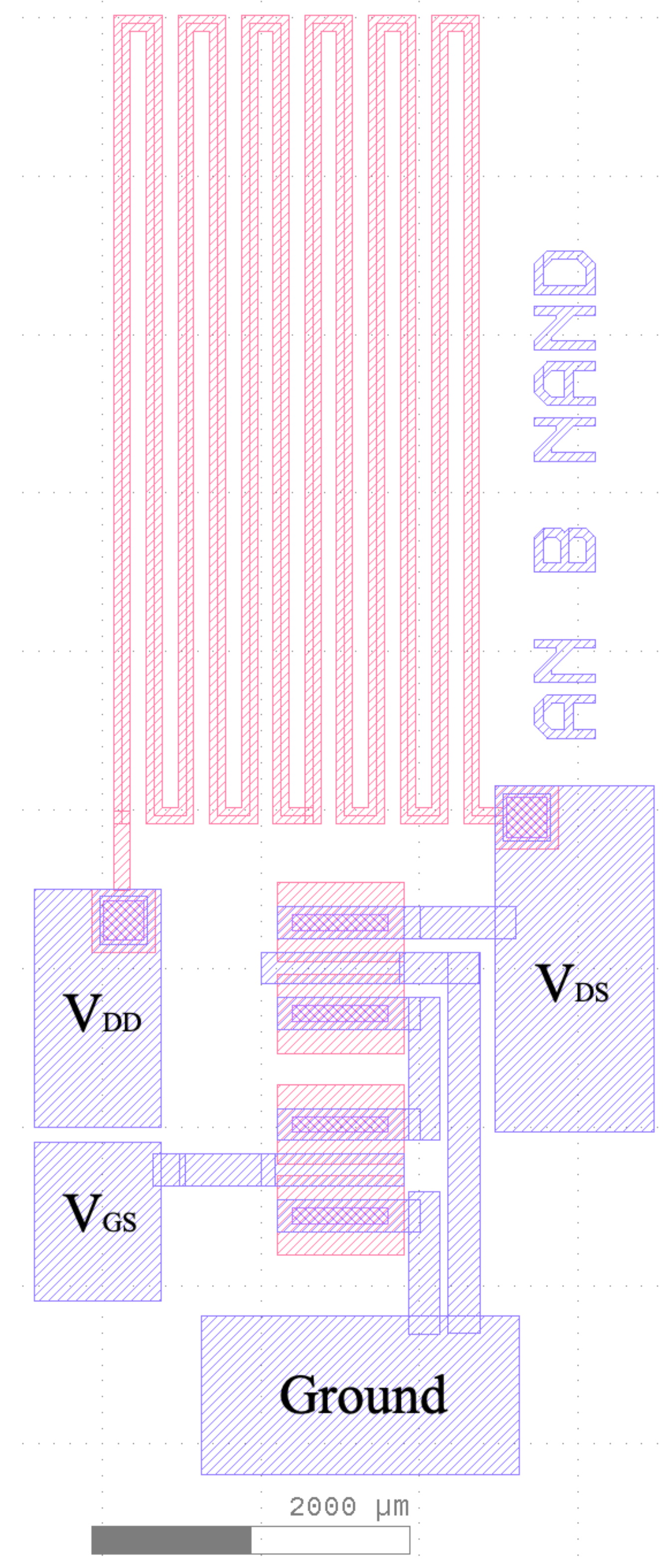


Figure 36: Close-up of the layout featuring the NAND gate with channel length of 75 µm.

Figure 37: Close-up of the layout featuring the OR gate with channel length of 75 µm.

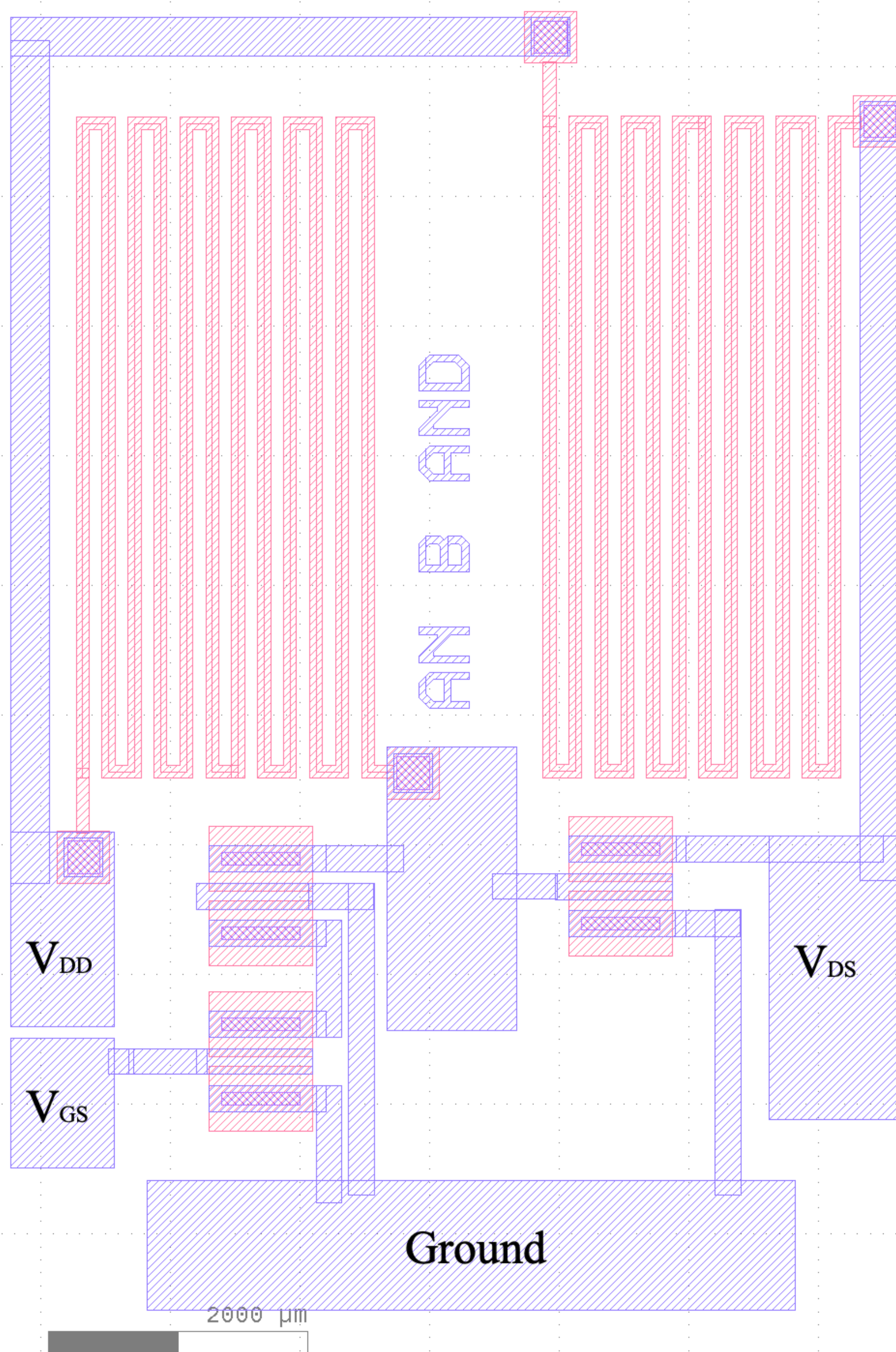


Figure 38: Close-up of the layout featuring the AND gate with channel length of 75 µm.

4.2 Transistor Parameters

The key foundation of the logic gate is the transistor. It is therefore critical to ensure proper functioning of the logic gate that the transistor, and all its parameters, are known and well characterized. Some important parameters would be the length of the channel L, the width of the channel W, the on current I_{on}, the off current I_{off}, the subthreshold swing (SS), the output resistance r_d, the on resistance R_{on}, the threshold voltage of the linear region V_{tlin}, the threshold voltage of the saturation region V_{tsat}, and the Drain Induced Barrier Lowering (DIBL).

The length and width of this transistor are 200 µm and 800 µm respectively. Figure 39 displays the length and width parameters on the transistor.

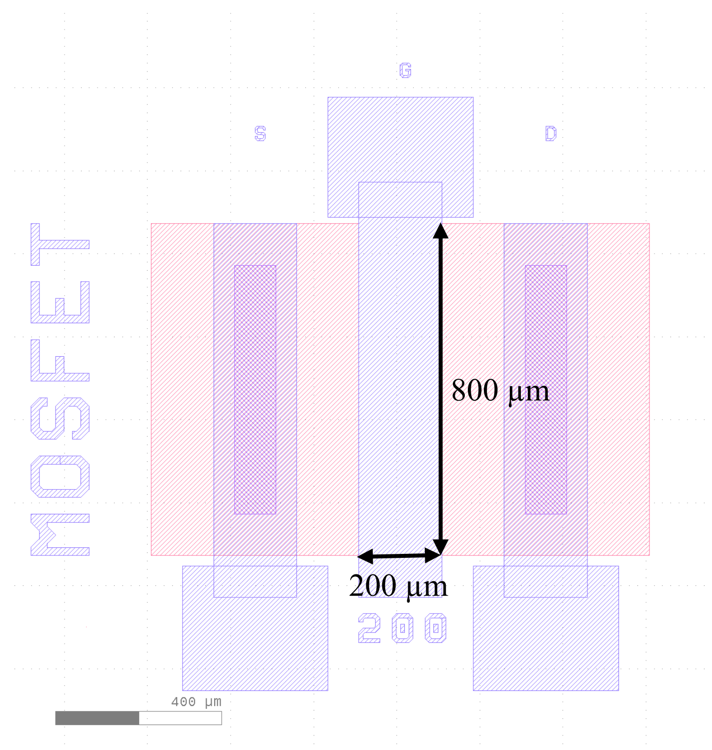


Figure 39: Illustration of the length and width of a typical transistor used in this work.

An isolated transistor from the NOT gate wafer was characterized. We used the LabTracer 2.0 software, two Keithley® 2400 Source Meter Units, three probes, and a stage. Figures 40 and 41 shows the setup for the hardware. The V_{DS} sweep ranged from through 10 V in steps of 0.35 V. The V_{GS} sweep ranged from -1 through 5 V in steps of 1 V. Figure 42 shows the current voltage graph. Figure 43 shows the transfer characteristic graph.

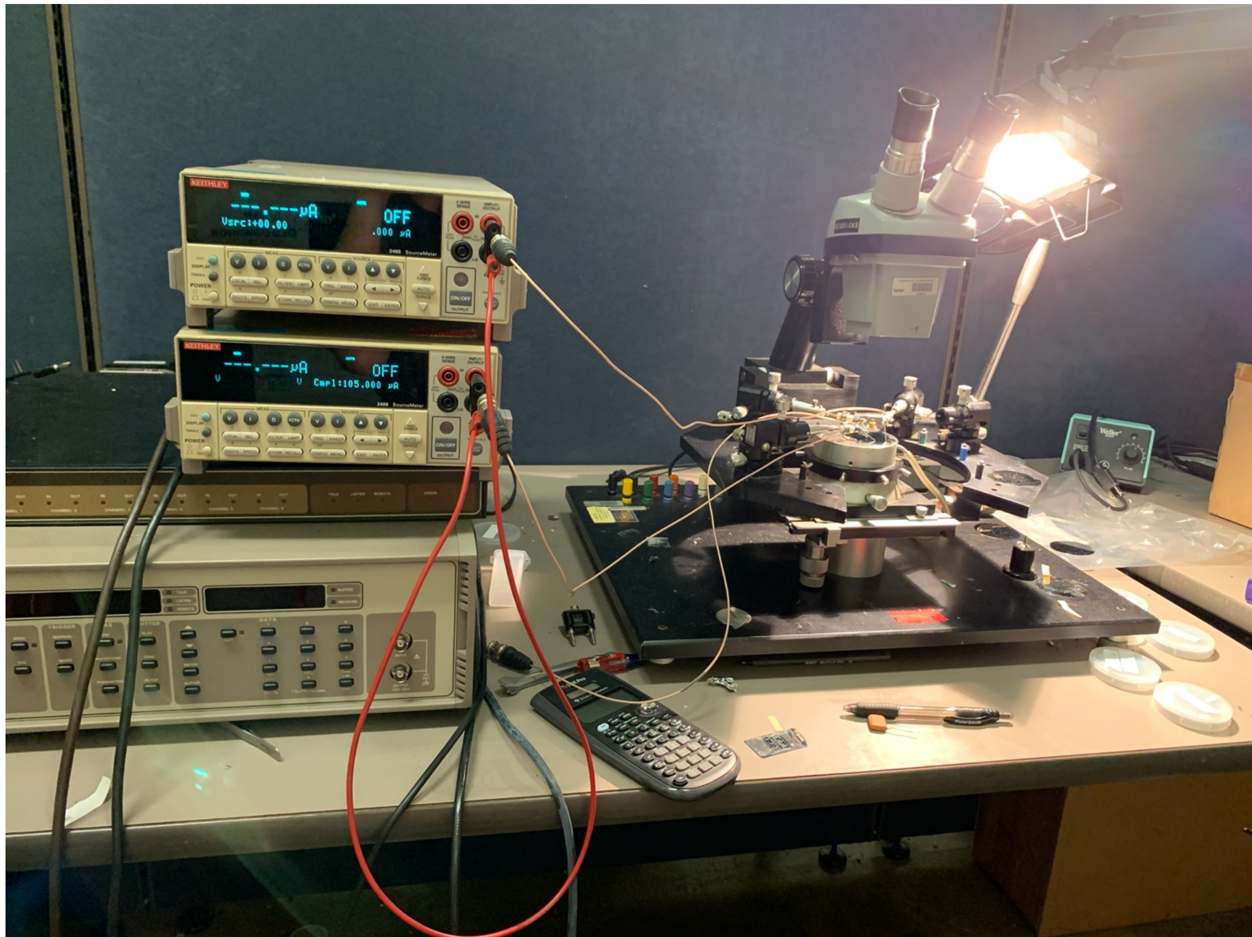


Figure 40: Set-up used to measure the transistor characteristics.

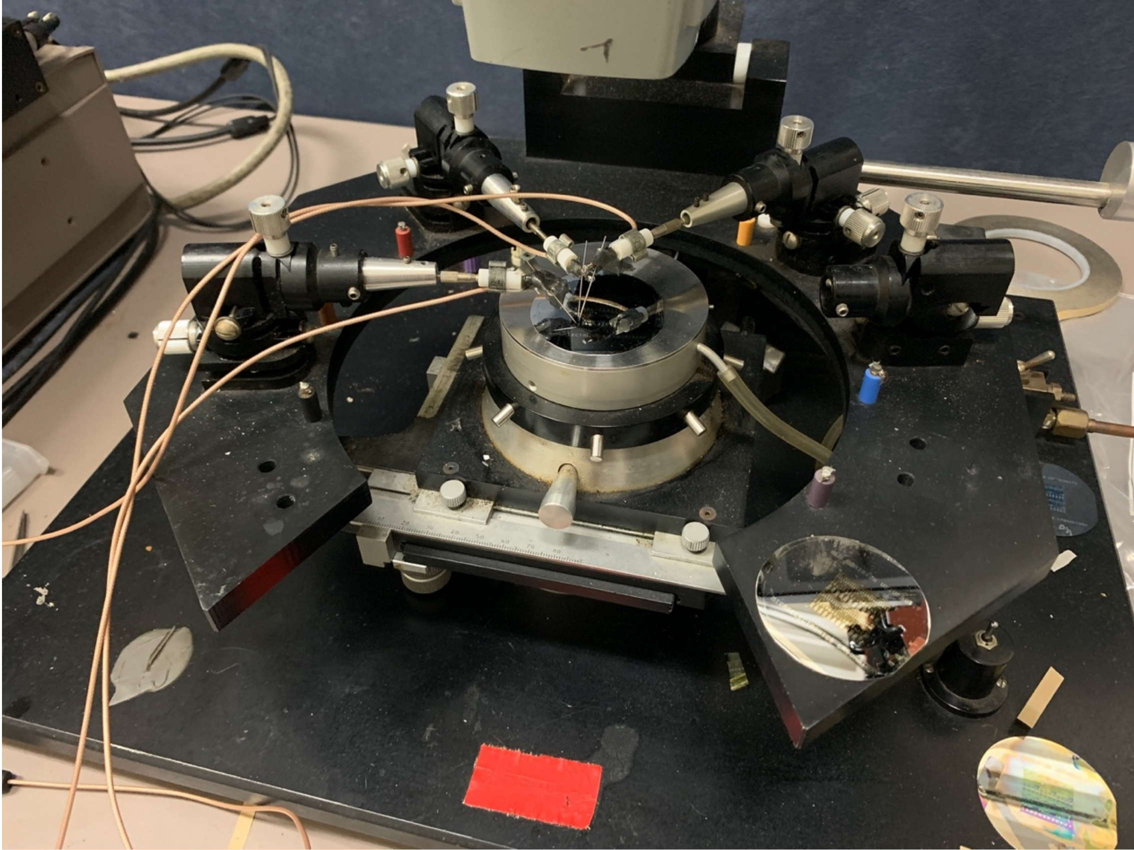


Figure 41: Close-up of the set-up used to measure the transistor characteristics.

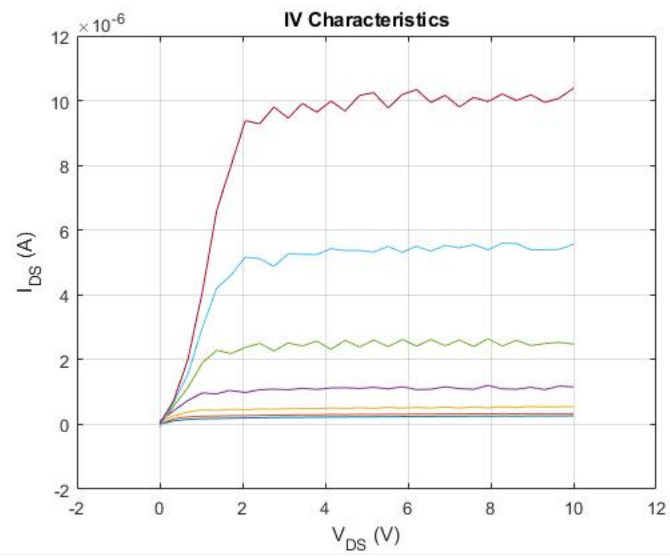


Figure 42: Typical I-V characteristics measured for a transistor used in this work.

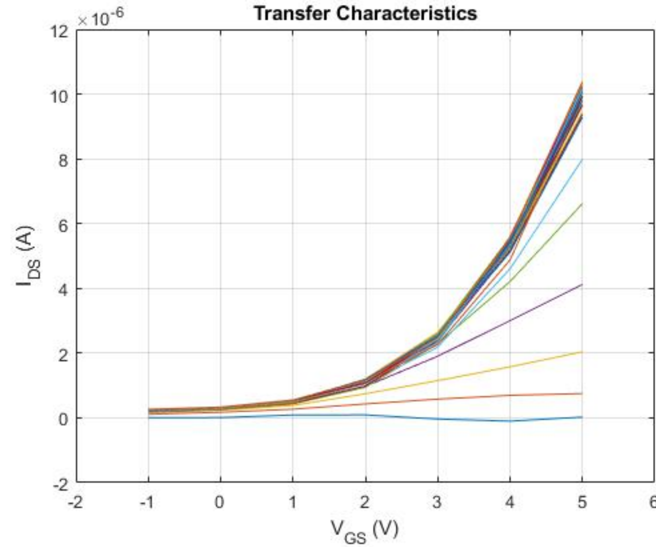


Figure 43: Typical transfer characteristics of a transistor used in this work.

Multiple parameters may require that $V_{GS} = V_{DS\ max}$, but since data was not gathered at $V_{GS} = 10$ V, so the value for $V_{DS\ max}$ will be 5 V instead of 10 V. I_{on} occurs at the maximum drain current I_{DS} when $V_{GS} = V_{DS\ max}$ [8]. When $V_{GS} = V_{DS\ max} = 5$ V, $I_{on} = 3$. I_{off} occurs when $V_{GS} = 0$ and $V_{DS} = V_{DS\ max}$ [8]. When $V_{GS} = 0$ and $V_{DS} = V_{DS\ max} = 5$ V, $I_{off} = 0.255$ µA.

SS is the amount the V_{GS} must increase in order for I_{DS} to increase by a factor of 10. Equation 1 is the formula to calculate SS [8]. When $V_{DS} = 5$ V, SS = 0.376 V/decade. SS is important, because reducing SS reduces I_{off}.

$$SS = \left[\frac{d(log I_{DS})}{dV_{GS}}\right]^{-1} \qquad (4.1)$$

r_d is the inverse of the slope of an IV curve in the saturated region [8]. r_d is usually measured when $V_{GS} = V_{DS\ max}$ [8]. Equation 2 is the formula for r_d [8].

$$r_d = \left[\frac{dI_{DS}}{dV_{DS}}\right]^{-1} \qquad (4.2)$$

We used MATLAB® to curve fit a line in the saturation region when $V_{GS} = V_{DS\ max} = 5$ V. Figure 44 shows the original line in blue and the curve fitted line in orange. The equation of the

curve fitted line was $f(x) = 4.2741\times10^{-8}x + 9.7466\times10^{-6}$. Taking the inverse of the slope gives r_d = 23.4 MΩ.

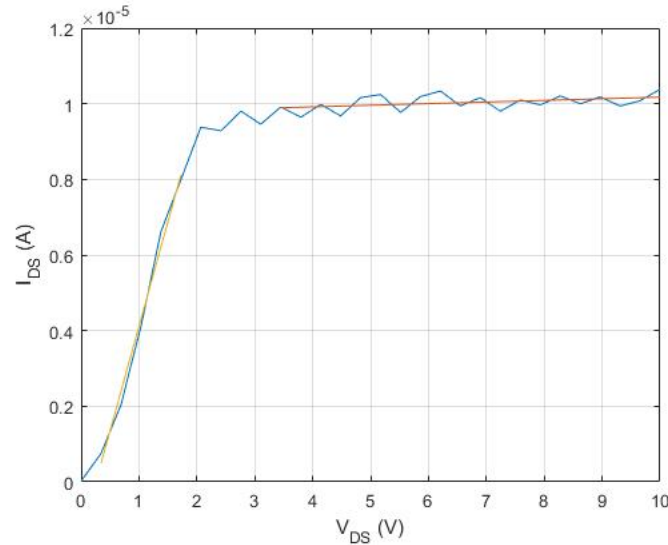


Figure 44: Graph illustrating the extraction of r_d and R_{on} from the data. The blue line is the original data, the orange line is a curve fitted line that is used to find r_d, and the yellow line is a curve fitted line that is used to find R_{on}.

R_{on} is the inverse of the slope of an I-V curve in the linear region when $V_{GS} = V_{DS\ max}$ [8]. We used MATLAB® to curve fit a line in the linear region when $V_{GS} = V_{DS\ max}$ = 5 V. Figure 44 shows the original line in blue and the curve fitted line in yellow. The equation of the curve fitted line was $f(x) = 5.5283\times10^{-6}x - 1.4142\times10^{-6}$. Taking the inverse of the slope gives R_{on} = 180.9 KΩ.

The threshold voltage must also be found. There is a threshold voltage for the linear region, and another in the saturation region [8]. The threshold voltages can be found on the transfer characteristic graph by picking a line corresponding to a particular V_{DS}, finding the steepest and straightest portion of the line, then drawing a new line that follows the slope of the original line in order to find the x-intercept. V_{tlin} is found by picking a line corresponding to a low V_{DS}, and V_{tsat} is found by picking a line corresponding to a high V_{DS}. Figure 45 shows both the original lines and the curve fitted lines to find the V_{tlin} and V_{tsat}. A low V_{DS} is represented with a blue line corresponding to V_{DS} = .35 V, but it is difficult to see due to the curve fitted orange line being so

close to the original blue line. The equation for the curve fitted orange line is $f(x) = 1.0782\times10^{-7}x - 2.3750\times10^{-7}$, which gives an x-intercept and V_{tlin} of -2.2 V. A high V_{DS} is represented with a violet line corresponding to V_{DS} = 5 V, and the curve fitted line is represented with a green line. The equation for the curve fitted orange line is $f(x) = 3.8174\times10^{-6}x - 9.2122\times10^{-6}$, which gives an x-intercept and V_{tsat} of 2.4 V.

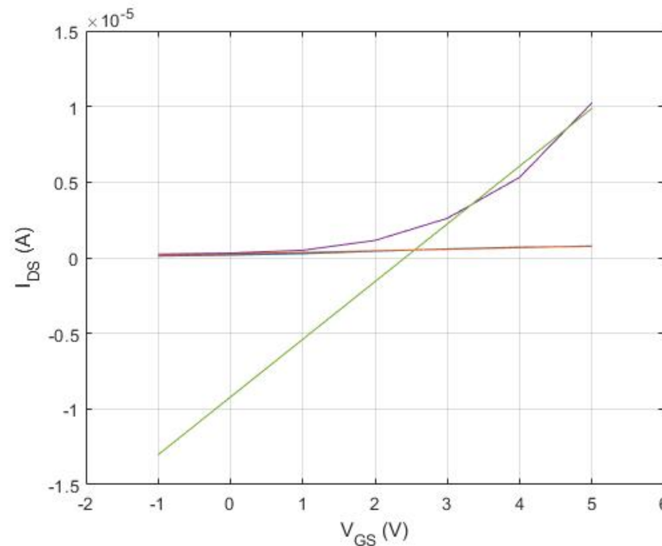


Figure 45: Graph illustrating the extraction of the threshold voltage from the data.

Drain induced barrier lowering (DIBL) is found by the change in V_{GS} over the change in V_{DS} at the same I_{DS} in the subthreshold region. Equation 3 is the formula for DIBL.

$$DIBL = \frac{dV_{GS}}{dV_{DS}} \quad (4.3)$$

We were unable to estimate the value for DIBL, because the lines representing the higher V_{DS} values are curvy, while the lines representing the lower V_{DS} are straight at the same I_{DS}. By the time the lines representing the higher V_{DS} become straight, the lines representing the lower V_{DS}

are above threshold, and DIBL must be calculated below threshold. Figure 46 shows the semilog transfer characteristic graph where the range of V_{DS} is 0.35 V through 5 V.

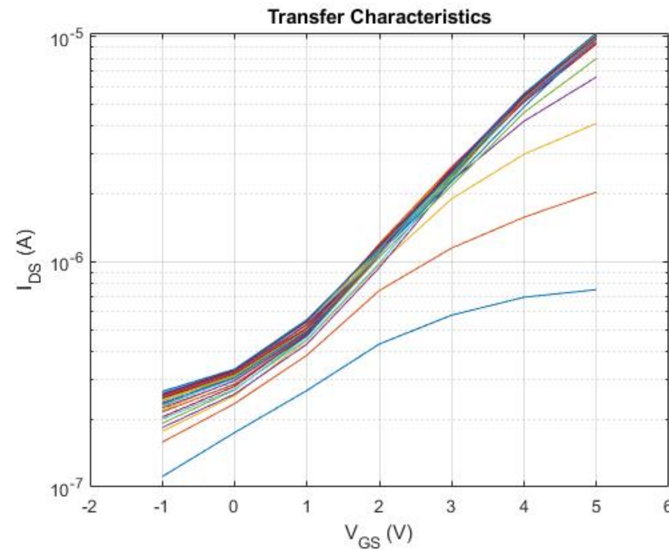


Figure 46: Graph illustrating the extraction DIBL from the data.

4.3 Logic Gates

Logic gates are the fundamental building blocks for all digital systems. They are generally built with MOSFET transistors. A specific name is given to each gate to help describe the specific function to be carried out by the gate. In the following section, we present the results on the logic gates we fabricated.

4.3.1 NOT Gate Wafer Characterization

Several NOT gates from the NOT gate wafer were characterized. The software used was the LabTracer 2.0 software, two Keithley® 2400 Source Meter Units, a digital multimeter (DMM), five probes, and a stage. Figure 47 shows the setup for the hardware. There were only probe mounts for three of the probes, so the other two probes were supported by other miscellaneous objects

assembled together to form improvised probe mounts. The probes supported by the improvised probe mounts were connected to a DMM, which measured V_{DS}. Despite the layout having many combinations of transistor gate lengths and resistors, only two NOT gates were characterized. Originally, there were only three probes, which would be placed on the source, gate, and the other end of the resistor which was not the drain, and V_{DS} would have been calculated using a voltage divider circuit instead of being measured. The improvised probe mounts lacked the ability to fine tune the probes' position. Thus, only two NOT gates were characterized. One NOT gate had a channel length of 200 µm and the largest resistor. The other NOT gate had a channel length of 75 µm and the largest resistor. For the 200 µm gate, the V_{DD} sweep ranged from 0 through 15 V. The V_{GS} sweep ranged from 0 through 41 V. For the 75 µm gate, the V_{DD} sweep ranged from 0 through 10 V. The V_{GS} sweep ranged from 0 through 41 V.

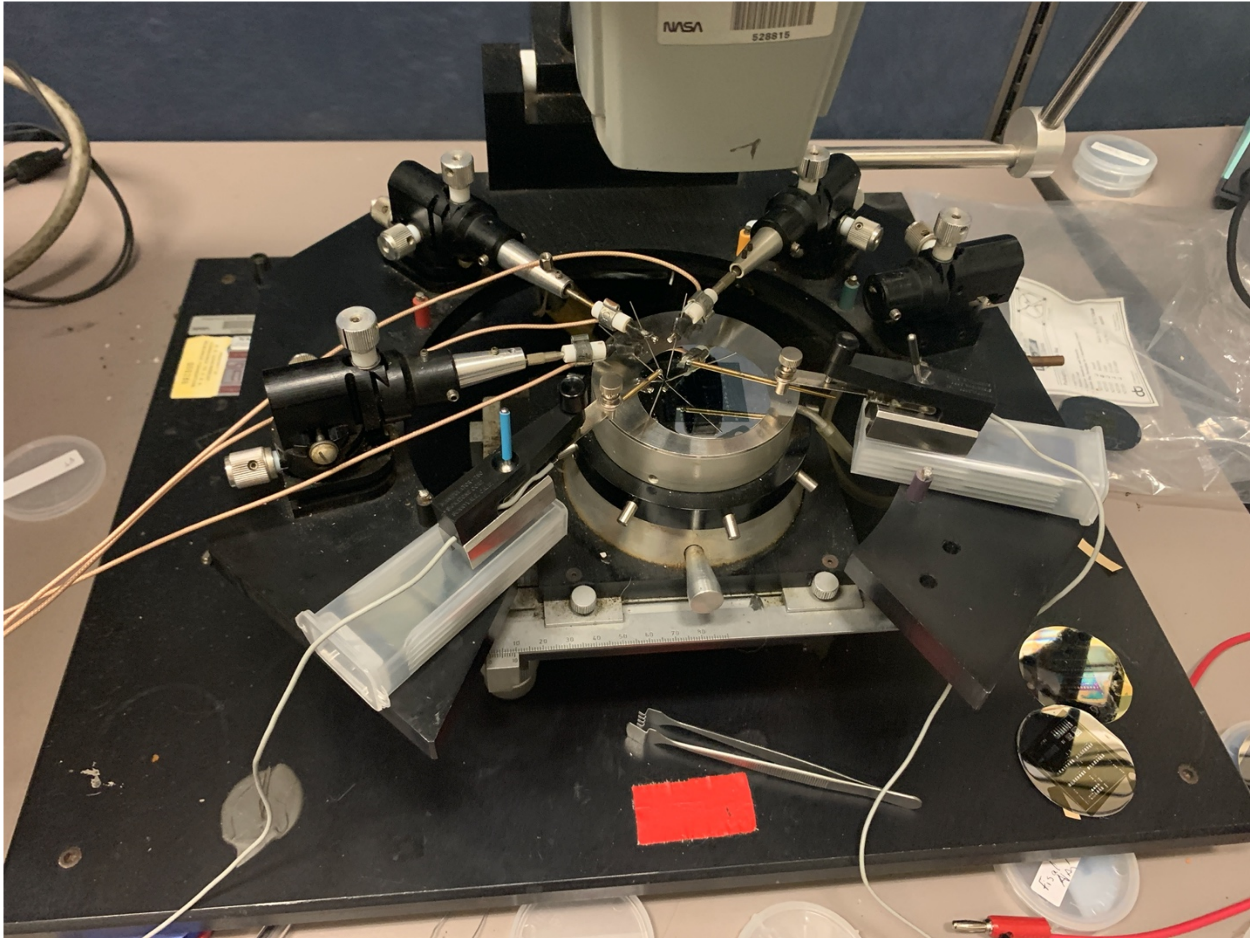


Figure 47: Hardware setup for characterizing the NOT gates. An extra pair of probes resting on improvised mounts were connected to a DMM to measure V_{DS}.

Figure 48 is the I_{DS} vs V_{DS} graph and Figure 49 is the Voltage Transfer Characteristic (VTC) graph for the logic gate with a channel length of 200 μm.

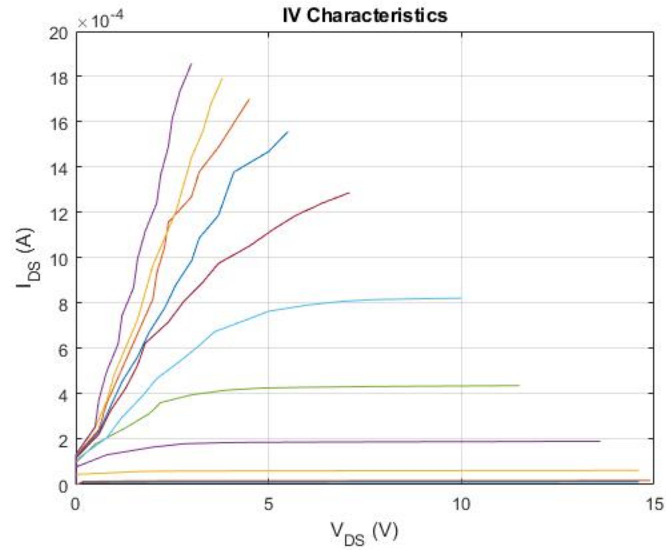


Figure 48: I_{DS} vs V_{DS} graph for the NOT gate with a channel length of 200 μm and the largest resistor.

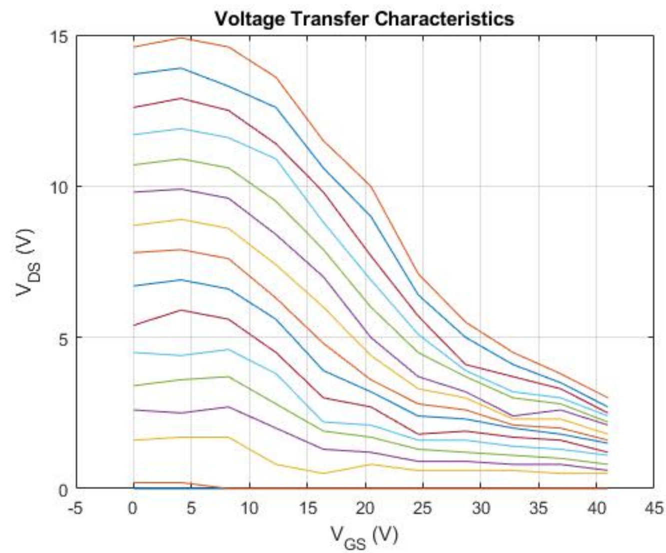


Figure 49: VTC graph for the NOT gate with channel length of 200 μm and largest resistor.

Figure 50 is the I_{DS} vs V_{DS} graph and Figure 51 is the (VTC) graph for the logic gate with a channel length of 75 μm.

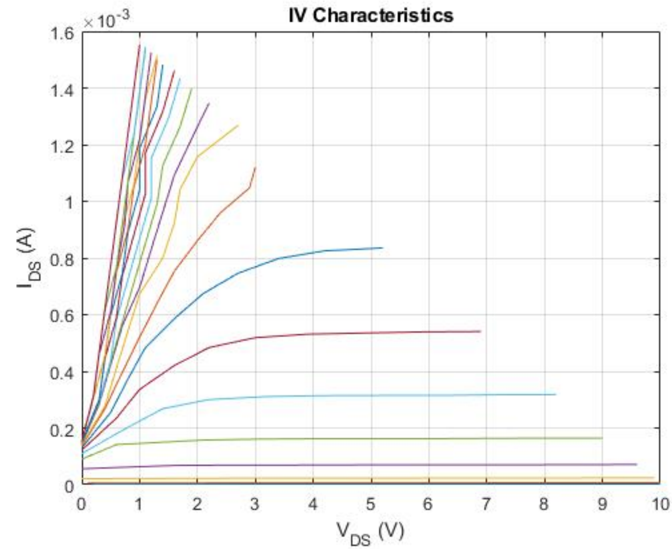


Figure 50: I_{DS} vs V_{DS} graph for the NOT gate with a channel length of 75 µm and the largest resistor.

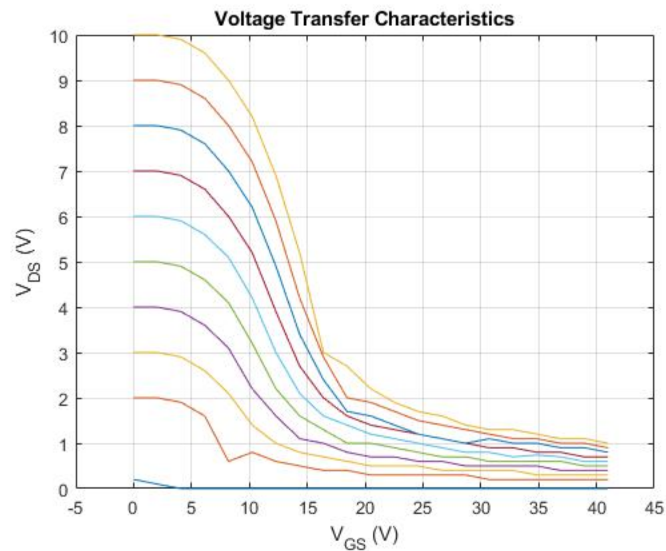


Figure 51: VTC graph for the NOT gate with channel length of 75 µm the largest resistor.

Figure 52 is a typical VTC graph [4]. The VTC graphs for the NOT gates with 200 µm and 75 µm channel lengths look similar to the typical VTC graph but shifted to the right. This may be caused by parasitic capacitances and parasitic resistances.

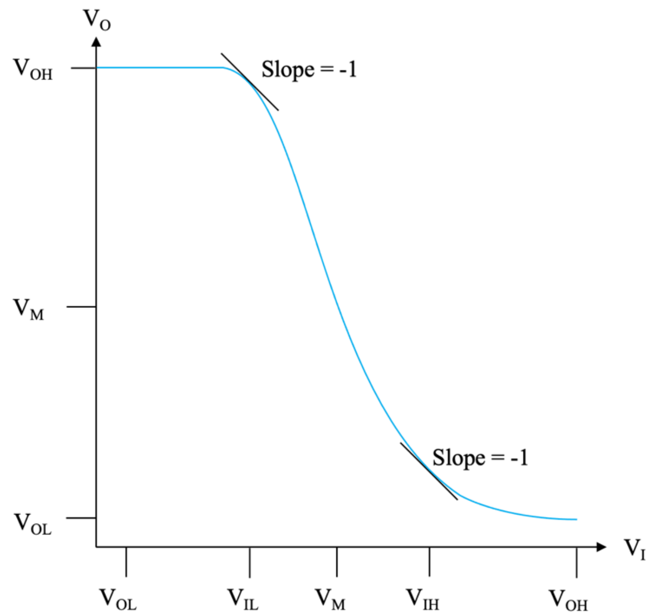


Figure 52: A typical VTC graph for a NOT gate [4].

The VTC graph for the logic gate with a channel length of 75 µm looks much more similar to the ideal VTC graph (owing probably a lower R_{on}), so the next logic gates are based on MOSFETs with a channel length of 75 µm and the largest resistor length, which is about 6 kΩ. A smaller channel length means there is less resistance in the transistor, which means a smaller voltage drop over the transistor. A larger resistor would also mean that the voltage drop across the resistor would be much more compared to the voltage drop across the transistor, so that is why the largest resistor is used. It is easier to distinguish between the HIGH and LOW output voltages when the difference between them is larger.

4.3.2 Other Logic Gates tested with 75 µm Gate

More NOT gates were tested in more detail. V_{out} was both calculated from I_{DS} vs V_{DS} measurements and directly measured with a digital multimeter (DMM). The resistor in the logic gate was calculated to be 6.5 kΩ. Figure 54 shows the blue line that is the measured data and the orange line that is the curve fitted to the straightest portion of the blue line in order to find the value of the resistor.

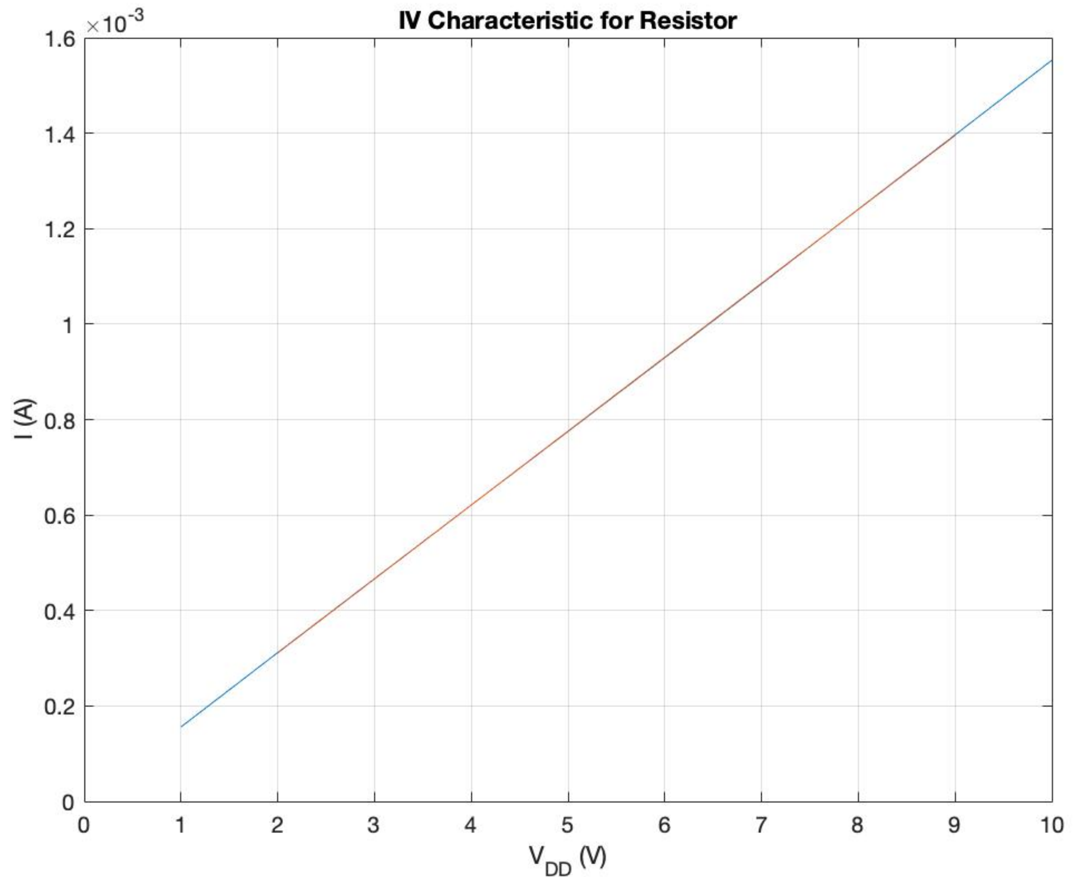


Figure 53: The I-V characteristic for the resistor used.

Then, R_{on} and R_{off} need to be calculated. When $V_{DD} = 4$ V and $V_{GS} = 0$ V, the measured current I was $2.82*10^{-6}$ A. Dividing V_{DD} by I gives $R_{off} = 1.4M\Omega$. When $V_{DD} = 4$ V and $V_{GS} = 10$ V, the measured current I was $3.00*10^{-4}$ A. Dividing V_{DD} by I gives $R_{on} = 13.3k\Omega$. $V_{GS} = 10$ V so that the difference between the HIGH and LOW V_{out} values are more noticeable compared to using a smaller V_{GS}. A voltage divider circuit is then used to calculate V_{out}. Equation 4.4 is the voltage divider equation where V_{DD} is the voltage source, R_R is the resistance of the resistor, R_{trans} is the resistance of the transistor, and V_{out} is the output voltage. When $V_{GS} = 0$ V, the value for R_{trans} becomes R_{off}, and when $V_{GS} = 10$ V, the value for R_{trans} becomes R_{on}.

$$\frac{V_{dd}R_{trans}}{R_R + R_{trans}} = V_{out} \qquad (4.4)$$

When $V_{GS} = 0$ V, the calculated output is $V_{out} = 3.98$ V. When $V_{GS} = 10$ V, the calculated output is $V_{out} = 2.69$ V. Ideally, when $V_{GS} = 10$ V, V_{out} would be less than 2 V, but there is at least a noticeable change in values when V_{out} goes from HIGH to LOW. Due to the R_{on} being so large and requiring more voltage to be dropped across the transistor, the voltage range for a LOW output is 0 V to 3 V, and the voltage range for a HIGH output is 3 V to 4 V.

When $V_{GS} = 0$ V, the measured V_{out} was 4.0 V. When $V_{GS} = 10$ V, the measured V_{out} was 2.2 V.

The NOR gate with the 01 input was tested. V_{out} was both calculated from IV measurements and directly measured with a digital multimeter (DMM). The resistor in the logic gate was calculated to be 13.4 kΩ. Figure 54 shows the blue line as the measured data and the orange line is curve fitted to the straightest portion of the blue line in order to find the value of the resistor.

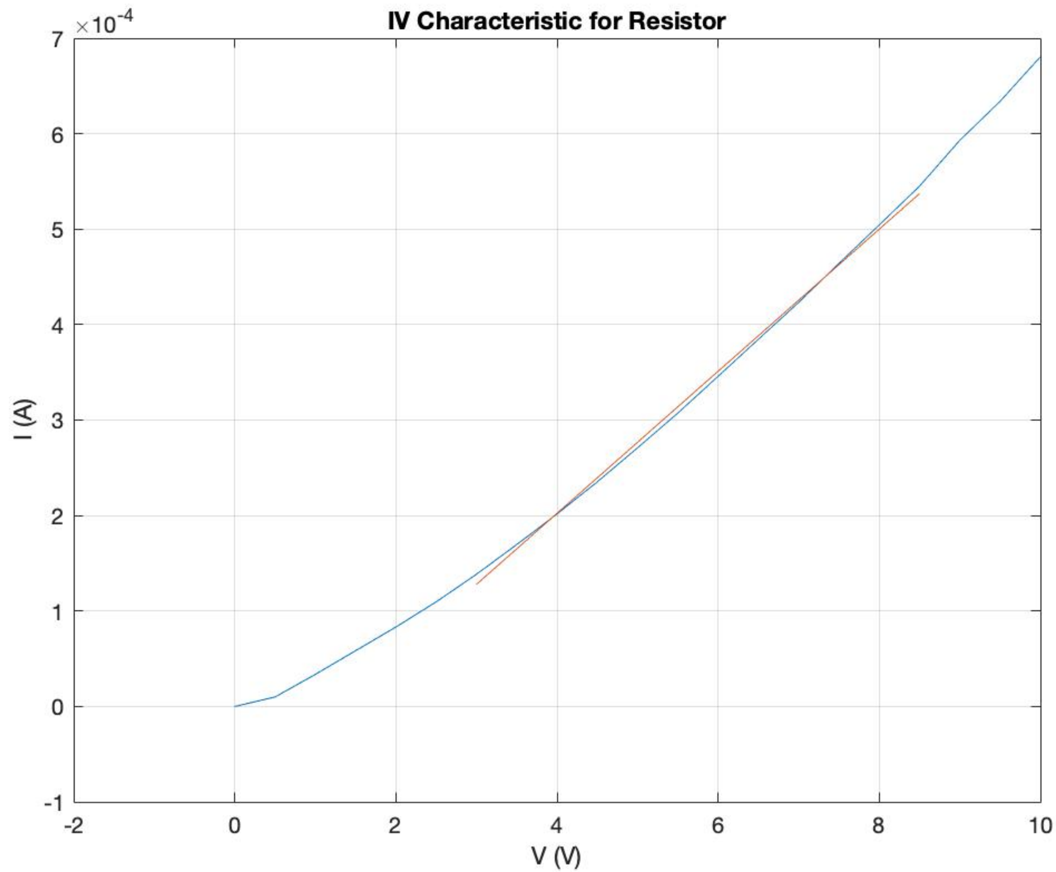


Figure 54: The IV characteristic for the resistor.

When V_{GS} = 10 V, the overall resistance of the NOR gate was calculated to be 41.1 kΩ. Figure 55 shows blue line is the measured data and the orange line is curve fitted to the straightest portion of the blue line in order to find the value of the overall resistance of the circuit. The resistor resistance is then subtracted from the overall resistance in order to find the resistance of the transistors in parallel, which is 27.7 kΩ.

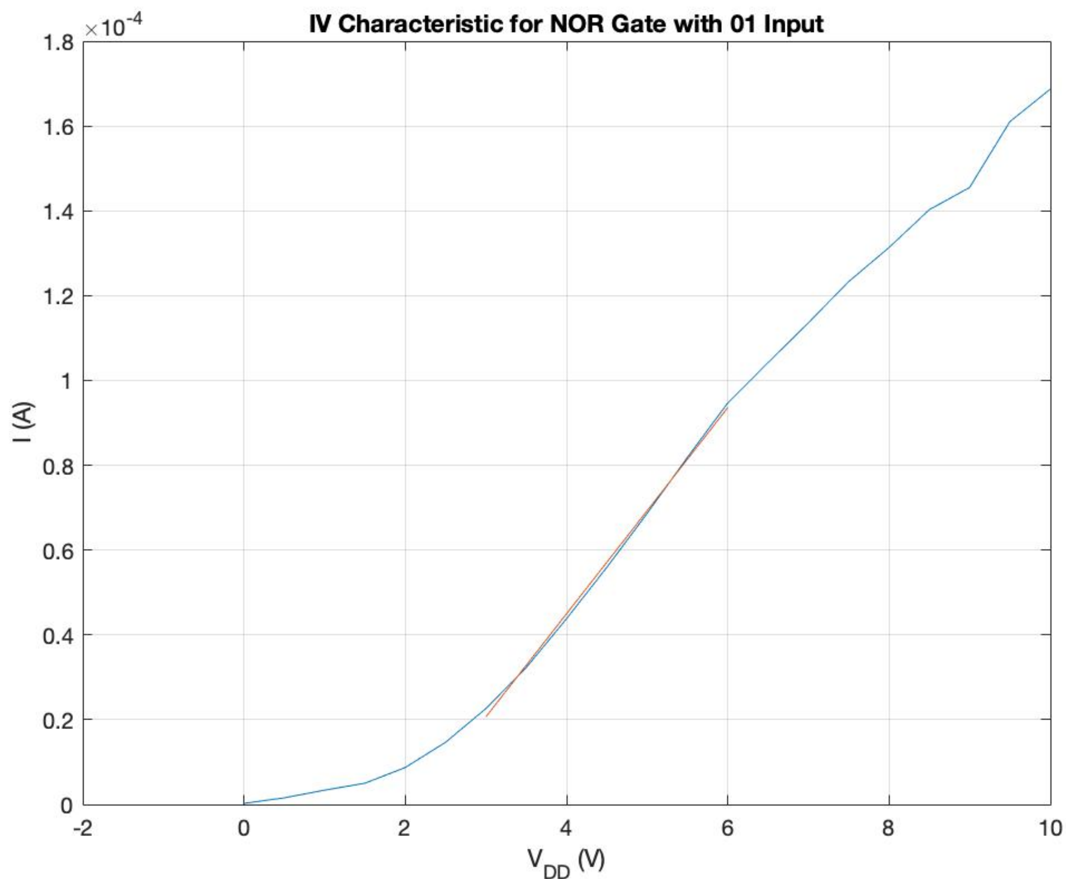


Figure 55: The IV Characteristic of the NOR gate with the 01 input.

A voltage divider circuit is then used to calculate V_{out}. Equation 4.4 is the voltage divider equation where V_{DD} is the voltage source, R_R is the resistance of the resistor, R_{trans} is the resistance of the transistors in parallel, and V_{out} is the output voltage. When V_{DD} = 4 V and V_{GS} = 10 V, the V_{out} calculated is 2.70 V.

We also tested the 01 input for the NOR gate with a V_{GS} = 0 V, effectively turning it into a 00 input for the NOR gate. The resistor value remains the same at 13.4 kΩ. When V_{GS} = 0 V, the overall resistance of the NOR gate was calculated to be 530.9 kΩ. Figure 56 shows that the blue

line is the measured data and the orange line is curve fitted to the straightest portion of the blue line in order to find the value of the overall resistance of the circuit. The resistor resistance is then subtracted from the overall resistance in order to find the resistance of the transistors in parallel, which is 517.5 kΩ.

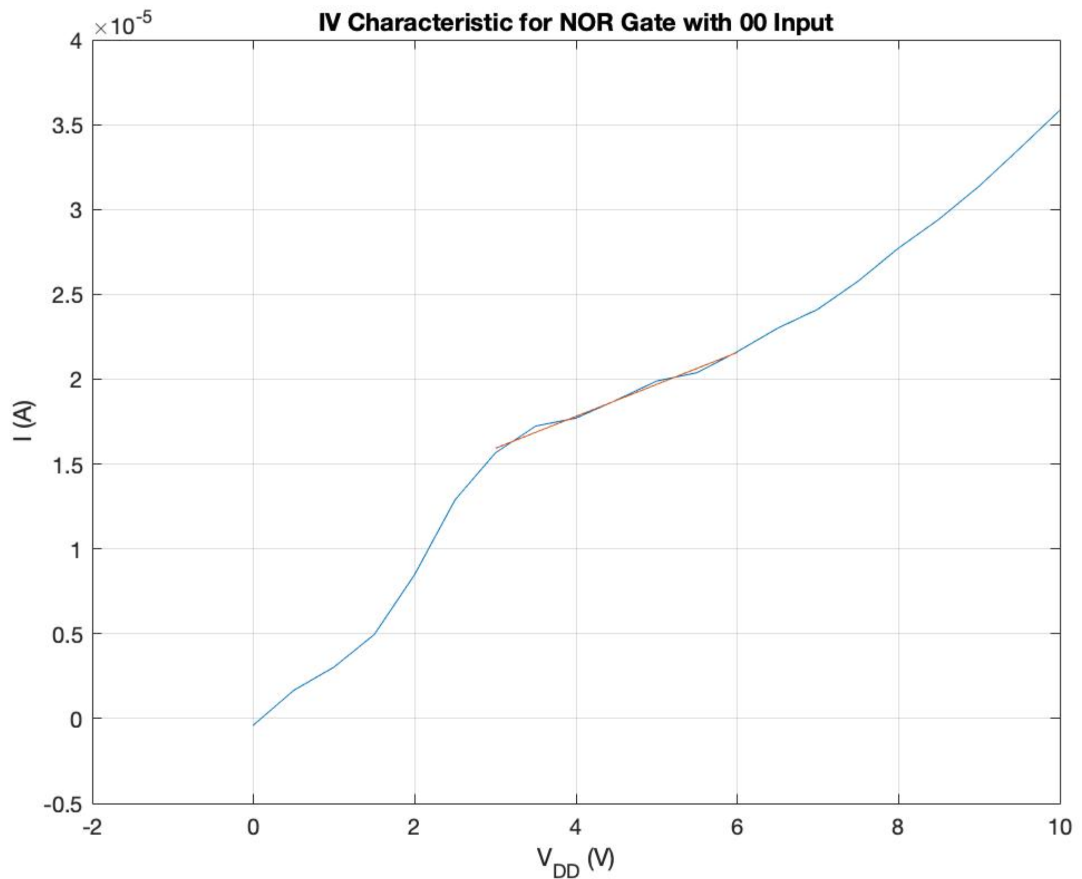


Figure 56: The IV Characteristic of the NOR gate with the effective 00 input.

When V_{DD} = 4 V and V_{GS} = 0 V, the V_{out} calculated is 3.90 V.

Due to the R_{on} being so large, the voltage range for a LOW output is 0 to 3 V, and the voltage range for a HIGH output is 3 to 4 V.

The output voltage was also measured with a DMM. When V_{DD} = 4 V, V_{GS} = 0 V, V_{out} = 3.22 V. When V_{DD} = 4 V, V_{GS} = 10 V, V_{out} = 2.31 V. This demonstrates that the NOR gates are working.

Similar measurements were done on all the other gates (AND, OR, NAND) and positive results were found there too. Similar issues were observed, where the R_{on} resistance was slightly too large to simulate ideal gates, but small enough to distinguish between a logic HIGH and a logic LOW.

CHAPTER 5. CONCLUSION

NMOS logic gates were a predecessor to the CMOS logic gates widely used today. They allow for easier process steps and take into account the limited equipment that is available in the ODU clean room. We notably do not have an ion implanter, which prevents us at this stage to make a n-well easily. We also are doping mostly with phosphorous, as we are using a NMOS technology, and therefore have not developed yet any PMOS related technology, such as doping with boron. In this thesis, NMOS logic gates were studied in order to open a new field of research into logic gates at Old Dominion University. This work focuses mostly on the designs of the mask patterns and the design of the fabrication process. Because no prior work had ever been done at ODU on the fabrication of logic gates, we had to start designing the masks as well as all the processes from nothing. NOT, NOR, NAND, OR, and AND gates were fabricated with transistors with several gate lengths, but we ended up using a 75 µm gate length at it seems the most performant length. All gates fabricated demonstrated the expected behavior but with some limitations. Due to a high value on the on resistance for the transistor (R_{on}), the voltage divider between the on and off state of the transistor is not as distinguishable as in our simulations. This leads to a voltage range for the LOW or HIGH outputs to be narrower than anticipated, at 0 to 3 V and 3 to 4 V respectively. Future designs of the NMOS logic gates should work towards reducing the R_{on} value. Methods include increasing the dopant concentration and reducing the channel length. In the future, gate performance should be tested with step signals to assess the switching speed.

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