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Role of surface morphology in wafer bonding

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The strain patterns detected by x-ray topography in wafers bonded for silicon-on-insulator (SOI) technology were found related to the flatness nonuniformity of the original wafers. Local stresses due to the bonding process are estimated to be about 1×10^8 dynes/cm^2. The stress is reduced about 100 times for the thin (0.5 μm) SOI films. Most of the wafer deformation occurs during room temperature mating of the wafers. The deformation is purely elastic even at 1200 °C. The magnitude of the stress appears insignificant for complimentary metal-oxide-semiconductor devices performance.

I. INTRODUCTION

Intrinsic wafer bonding, with no adhesive layer applied between two mated surfaces, has been extensively studied for silicon-on-insulator (SOI) applications.[1] It has been reported that the bond strength between two wafers, i.e., the density of individual chemical bonds established between the surfaces, expressed in terms of specific surface energy, monotonically increases with bonding temperature.[2,3] Since the wafer surfaces are never perfectly smooth, the bonding process has to deform each wafer in order to achieve conformity of the two surfaces. This deformation and its relation to surface morphology is the subject of this study.

Two sufficiently smooth, flat, and hydrophilic oxides can spontaneously form a bond at room temperature (RT).[3] Prime quality silicon wafers, oxidized or not, despite their flatness variation of several micrometers, or surface microroughness of several angstroms, can be easily mated. The bond strength, measured using a method based on crack propagation theory,[3] can be subsequently increased at elevated temperatures up to the cohesive (bulk) energy of thermal oxide (a complete fusion of the oxides). Part of the bonding process is facilitated through deformation of the wafers both macroscopically, to accommodate nonflatness, and microscopically, to overcome local roughness.[2,3]

In typical SOI applications, one or both of the wafers are covered with thermally grown oxides. In our experiments both wafers in each pair were oxidized to the same thickness. Except as noted, a 300-nm thermal oxide was grown in steam on all our samples, 4-in. Si (100) wafers.

II. WAFER DEFORMATION VS SURFACE TOPOGRAPHY

X-ray topography (XRT), known for its high sensitivity to local strains in monocrystalline materials, was used to image the bond. Samples bonded at room temperature, 200, 800, and 1200 °C were examined. The images clearly delineate the boundary of bonded areas and define the unbonded "voids." Wafer deformation gives rise to a contrast change due to local variations in the Bragg condition which can increase or decrease the diffracted beam intensity. The deformation is illustrated in the x-ray transmission topographs in Fig. 1. The large dark area in the left lower corner of the image of Fig. 1(a) indicates wafer warpage caused by the conformation of each of the wafers to the other's nonflatness. The magnified image in Fig. 1(b) shows the roughness-like pattern present throughout the bonded area of a wafer. Its largest components have a spatial wavelength of the order of 1 mm, and will subsequently be referred to as "waviness."

It has been recently suggested,[1,4] that the observed waviness contrast is related to variations in the local flatness of the wafers. In order to find a correlation of the observed XRT pattern with the original topography of the bonded surface, the roughness of one of the bonded wafers, whose XRT is shown in Fig. 1(b), was measured using an optical profilometer after the wafer was separated from its mate. Figure 2(a) shows a three-dimensional profile of the surface of the wafer. The amplitude and spatial frequency distribution of the roughness' sinusoidal components are illustrated in Fig. 2(b). Both representations indicate that the dominant component has a spatial wavelength of the order of 1 mm, i.e., comparable to that observed in x-ray topographs.

When two surfaces of similar topography adhere together, the periodicity of the strain pattern resulting from the pushing forces (at the asperities) and the pulling forces (in the valleys) should be comparable to that of the original surface roughness periodicity. Hence, the waviness contrast observed in x-ray topography is directly related to the waviness of the bonded surfaces. Consequently, the local regions where the wafers remain unbonded appear

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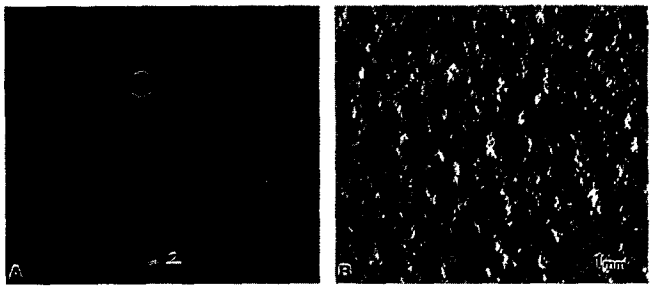

FIG. 1. X-ray topographs showing the strain contrast introduced between two silicon wafers bonded at 800 °C, (a) full 4-in. wafer image showing warpage in lower left corner (wafers unoxidized), and (b) 10× magnified image of a strain pattern related to the wafer surface waviness (300 nm of SiO_2 on each wafer).

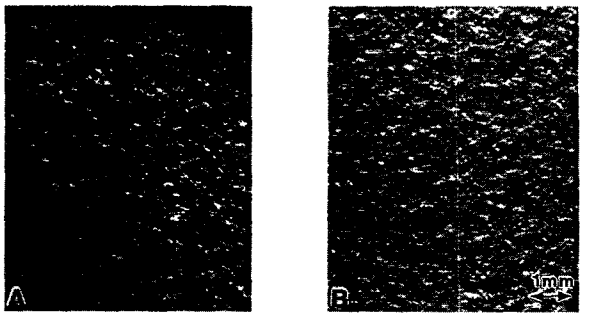

FIG. 3. X-ray topographs of wafer pairs bonded at (a) RT, and (b) 1200 °C for 10 min in N_2. The roughness-like strain contrast remains essentially unchanged indicating that most of the strain results from the RT bonding.

smooth, indicating that no strain variation is present there. This is clearly visible in the areas at the edge of the wafer and inside the large void of Fig. 1(a). The roughness characteristics may vary for wafers from different sources as polishing techniques change. X-ray topographs of the bonds between two wafers without thermal oxide films are essentially the same as for oxidized wafers, suggesting that only an insignificant amount of the stress is attenuated in the 300-nm-thick oxide.

The strain contrast in the x-ray topographs of bonds formed at higher temperatures (200, 800, and 1200 °C) does not show any appreciable difference from the RT bonded pair image (Fig. 3). This shows that most of the deformation of the wafers occurs during the initial mating of the wafers at room temperature. The deformation of the wafers during bonding can be represented schematically, as in Fig. 4. The surface waviness is accommodated by room

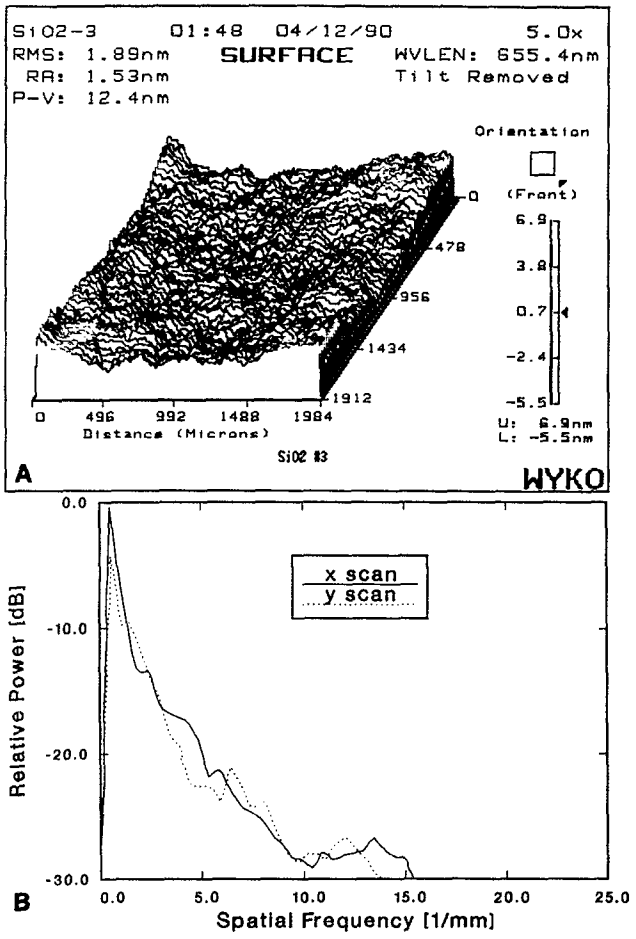

FIG. 2. Three-dimensional rendering of the wafer surface topography (a), and the distribution of the amplitude and wavelength of its spatial components (b), from optical profilometry. Spectra calculated for two orthogonal directions are shown in (b). The measurement was performed on the wafer of Fig. 1(b) after the bonded wafers were separated. Similar results were obtained when the measurement was taken after the oxide was stripped with HF.

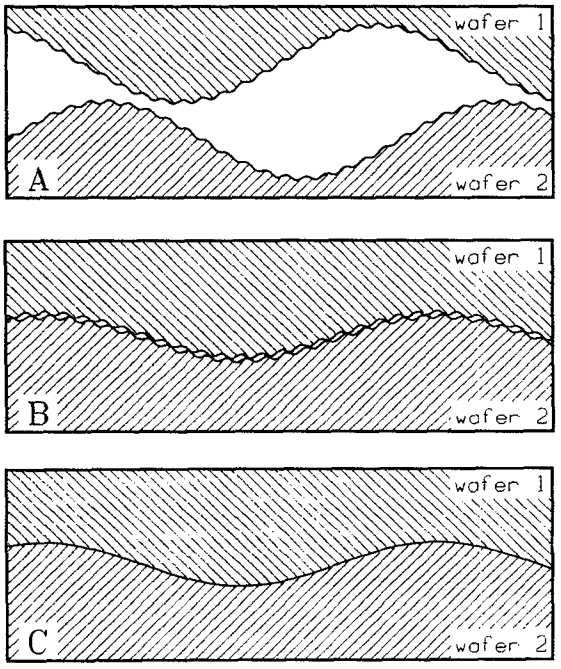

FIG. 4. Schematic representation of the deformation introduced by the bonding process: (a) wafers surfaces before bonding, (b) after RT bonding, and (c) after complete bonding at high temperature. For simplicity, only two sinusoidal components of the surface roughness are shown.

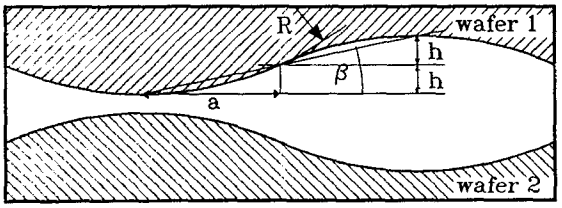

FIG. 5. Geometry of the surface waviness used in calculation of local stress due to bonding.

temperature bonding, rendering the surfaces much flatter [Fig. 4(b)] than before [Fig. 4(a)]. The contact area between the two surfaces is relatively low due to the roughness components of higher spatial frequency. Thus overall low bond strength results. Bonding at higher temperatures [Fig. 4(c)] involves formation of the Si—O—Si bond,[2,3] where the intermolecular forces have much shorter range than the hydrogen bond forces acting in the room temperature bonding. The wafers become bonded much more strongly, but the surface deformation caused by the process is much more localized. The associated contrast fluctuations are likely to be below the resolution of x-ray topography.

III. QUANTITY AND TYPE OF LOCAL STRESS

A. Stress in wafers

An attempt was made to evaluate the amount of local stress caused by the flattening of the rough surface. Assuming spherical geometry of the asperities and valleys, and using the highest stress case where the asperities of the two wafers are aligned with respect to each other, we have calculated the stress using the theory of deformation of elastic spheres.[5] A schematic illustration of the geometry of this model is shown in Fig. 5. The asperities and the valleys collapse a distance h onto a plane located half way between those containing the tips of the asperities and the bottoms of the valleys, respectively. The stress, normal to the surface and averaged over the asperity base area, is expressed by

$$\sigma_{\max}=4Eh/[\Pi a(1-\nu^2)], \tag{1}$$

where E is Young's modulus of silicon, ν is Poisson's ratio, and a is 1/4 of the spatial wavelength (or peak-to-peak distance). For a wavelength of 1 mm, $a=0.25$ mm. The average peak-to-valley height of the waviness, as evaluated from three 2×2 mm profilometer topographs of our samples, was about 20 nm; hence $h=10$ nm. Using the above equation we have $\sigma_{\max}\simeq1\times10^8$ dynes/cm^2. There are other prominent roughness components, with spatial wavelength, about ten times shorter than the waviness, visible both in the XRTs of Figs. 1(b) and 3, and in the optical profile spectrum of Fig. 2(b). However, according to the spectrum of Fig. 2(b), the amplitude of these components is more than a factor of ten smaller. Thus, $\sigma_{\max}$ evaluated for the waviness remains the largest local stress at the bond. The stress will be less for smoother surfaces, such as those shown in Fig. 3, where the large waviness component is much less pronounced than in Fig. 1(b). For comparison, Yamada *et al.*[4] reported a stress of 9×10^8 dynes/cm^2 (corrected here for $E=1.66\times10^{12}$ dynes/cm^2 used in our calculation) in their bonded samples, using the broadening of the (400) diffraction peak.

The stress varies from tensile to compressive throughout the wafer depending on local geometry of the mated surfaces.

B. Stress in thin films

As the device wafer of a bonded pair is thinned, it becomes more deformed by the relaxing substrate wafer. When the top silicon film becomes very thin, the stress in the substrate relaxes almost completely and its transmission x-ray topograph shows no waviness contrast.[4] This relaxation forces the device film to deform in the vertical direction a distance of another h at the extremities of the roughness profile. However, the increased elasticity of the thinned wafer is expected to lower the stress in the film. Because the thickness d of the film is now much smaller than the diameter $2a$ of the deformed area in consideration, the elastic spheres approach becomes invalid and a bending of a uniformly loaded thin circular plate model[6] will be used instead to calculate the stress.

Two cases are considered: first, a plate clamped at the edge (the edge is not allowed to move freely), and the second, a plate simply supported at the edge (movement is allowed). In the first case the maximum stress is present at the edge of the plate and can be expressed by

$$\sigma_{\max}=4Ehd/[a^2(1-\nu^2)]. \tag{2}$$

For the simply supported plate the maximum stress occurs at its center and is equal to

$$\sigma_{\max}=2Ehd(3+\nu)/[a^2(5+\nu)(1-\nu)]. \tag{3}$$

Assuming a fully relaxed substrate (h is twice as large as in the thick case considered above) and the silicon film of a typical thickness of 0.5 μm, the stress calculated with the help of Eq. (2) is equal to about 1.2×10^6 dynes/cm^2. Using Eq. (3) we obtain $\sigma_{\max}=4.4\times10^5$ dynes/cm^2. Since some rotation of the edge of the plate with respect to the rest of the film is likely to occur in our case, the actual stress is expected to be somewhere between these two values. Lack of the waviness contrast observed in the XRT image of the thinned wafer in the bonded pair[4] (a more sensitive double-crystal XRT did show some of the contrast[4]) appears in agreement with this substantial decrease in the estimated stress in the film.

Notice that the asperities and the valleys of the waviness are only a very small deviation from the flat surface. Their radius of curvature is $R\simeq a^2/2h$, and for the above parameters is about 3 m. The average slope angle is about $\beta\simeq0.002°$.

It is reassuring to notice that the stresses introduced by the bonding process are negligible in comparison to some other local stresses present in the immediate vicinity of the device active areas. For instance, the stress near the edge of a window in a deposited film is of the order of the built-in

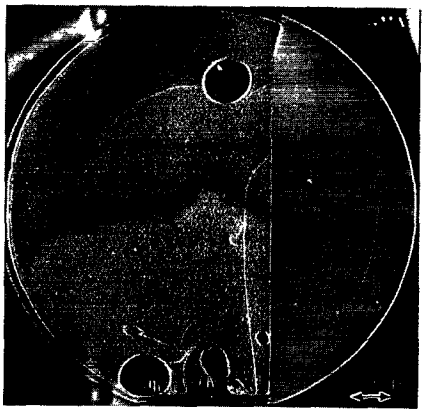

FIG. 6. X-ray topograph of a wafer pair bonded at 800 °C for 10 min in N_2. Part of one wafer in the pair was removed after bonding by cleaving. No roughness-like contrast is present in de-bonded part of the sample.

stress in the film,[7] which for typical thermal oxides on silicon is about 3×10^9 dynes/cm^2.[8]

C. Plastic deformation

By some estimates,[9] the stress necessary to spontaneously nucleate dislocations in an otherwise perfect crystal is equal to about 1/30 of the materials's sheer modulus, or $\simeq 2.5\times10^{10}$ dynes/cm^2 for silicon. Hence, bonding-induced stresses, which are several orders of magnitude lower, should not affect structural properties of the silicon film on the bonded-wafer SOI substrates. An experiment was performed to assess whether the observed bonding-induced deformation is indeed free of any plastic component. Three pairs of oxidized wafers were bonded at 200, 800, and 1200 °C, then each pair was cleaved along the bond over half of the wafer area, and one of the separated halves was broken off. X-ray topographs of the whole wafer in these samples show a perfectly smooth image of the uncovered surface, indistinguishable from the previously unbonded rim area of the wafer (Fig. 6). The bonded halves of the samples exhibit the familiar waviness contrast. We can conclude then, that the strain at the bond between two wafers has been released upon separation, thus implying the deformation was purely elastic. This is further confirmed by numerous cross-sectional and plan-view transmission electron microscopy observations,[3] where no bonding induced defects were seen.

D. Stress versus carrier mobility

Tensile stress is known to increase electron mobility and decrease hole mobility in silicon films; compressive stress causes the opposite effect.[10] As mentioned above, the bonding-induced stress in wafer-bonding SOI can be tensile or compressive at different wafer locations. However, the influence of the stress on the electrical parameters of the silicon film seems to be insignificant. Electron mobilities measured in nominally undoped, fully depleted CMOS transistors made in our bond-and-etchback SOI material were about 620 cm^2/V s for NMOS and 290 cm^2/V s for PMOS. The ratio of the two values for adjacent pairs of transistors varied little throughout the wafer, indicating negligible dependance on stress.

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