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Fabrication and Characterization of Silicon Field Emitter Arrays

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FABRICATION AND CHARACTERIZATION OF SILICON FIELD EMITTER ARRAYS

by

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ABSTRACT

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Field emission is a process through which the application of a large electric field to the surface of a material causes electron emission into vacuum. The electron emission current is a strong function of the geometry of the emitting material. The focus of this thesis is to investigate the effect of geometry on the emission current. Specifically, silicon field emitter arrays were fabricated using two separate fabrication processes termed the standard process and the new process. The uniformity of the arrays was measured experimentally. The arrays were used in field emission tests from which parameters controlling field emission were extracted. The results have shown that the new process gives the most uniform and consistent field emission performance.

ACKNOWLEDGMENTS

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CHAPTER I

INTRODUCTION

In general, there are four mechanisms responsible for the emission of electrons from the surface of a material into vacuum. These include thermionic emission, Schottky emission, photoelectric emission, and field emission. For thermionic, Schottky, and photoelectric emissions, the electrons gain sufficient energy from an external source to overcome the surface potential energy barrier of the material (i.e., the material's work function). Field emission is fundamentally different from these processes in that the surface potential barrier is made sufficiently thin through the application of a high electric field allowing the electron to pass through the barrier, rather than over it.

Thermionic emission utilizes elevated temperatures to supply the energy necessary for electrons to overcome the surface potential barrier. The high temperature induces large lattice vibrations in the emitting material. These lattice vibrations transfer energy to the conduction band electrons for emission. Schottky emission is similar to thermionic emission, using a combination of elevated temperature and an applied electric field. Again, as in thermionic emission, the high temperatures supply enough kinetic energy to the conduction band electrons to overcome the surface potential barrier. The addition of an electric field at the surface of the emitting material serves to reduce the height of the surface potential energy barrier. Hence, emission can occur at lower temperatures than required for purely thermionic emission. In photoelectric emission,

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energy is supplied to the electrons from photons striking the surface of the emitting material. If the energy of the incoming photon is greater than the surface potential energy barrier of the material, then an electron will be emitted. In the case of field emission, application of an electric field reduces the thickness of the material's surface potential energy barrier so that electrons near the surface can *tunnel* through the barrier rather than overcome it as in the other emission mechanisms. Hence, field emission is a quantum mechanical process. A detailed analysis of field emission is presented in chapter 2.

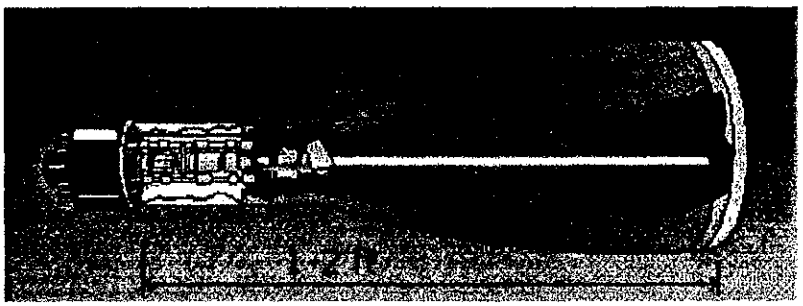
1.1 Applications of Field Emission

The drive for a "cheap" source of free electrons has lead to a vast amount of research devoted to the study of field emission. "Cheap" refers to the relative ease with which electrons are emitted by the process of field emission when compared to the other emission mechanisms. Field emission has a much smaller power requirement than thermionic and Schottky emissions since high temperature is not needed. In order to have a high photoelectric emission current, a large number of photons of high enough energy are required. Field emission is unquestionably 'cheaper' than this process since high electric fields are easier to create than a large number of photons at the appropriate energy.

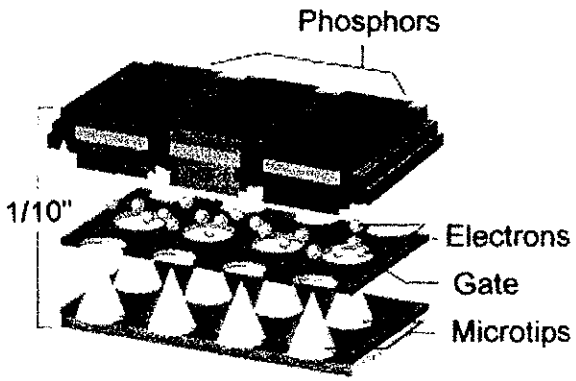
In addition to the relative ease with which electrons are emitted by the process of field emission, the emission area can be made quite large while maintaining a very thin cross-section. For this reason, the most promising application of field emission is the field emission flat panel display (FEFPD). A FEFPD would exhibit all the excellent display properties of the cathode ray tube (CRT) such as high brightness and contrast,

fast response speed, flat screen, and wide viewing angle, but would only require a fraction of the depth of a CRT display and have a much lower power consumption. Further, FEFPDs would have addressable pixels making them ideal as a digital display device.

Figure 1.1 is a cross-section representation of a CRT display and a FEFPD presented to illustrate the extreme reduction in depth of the FEFPD over the CRT display. In the CRT display, the process of thermionic emission is used as an electron source. The emitter is a filament (whose temperature is raised by resistive heating) that acts like a point source of electrons. The emitted electrons are shaped into a narrow electron beam, which must be scanned across a phosphor screen to create an image. Hence, the filament must be located at a large distance from the screen so that the beam can be scanned over the entire display area. In the FEFPD, the electron emitting area is spread over the entire area of the display. This allows each pixel in the display to have its own electron beam, eliminating the need to scan a single electron beam across the entire screen. Therefore, the depth of the FEFPD is only a fraction of the depth required by the CRT display.



Cathode Ray Tube



Field Emission Flat Panel Display

Figure 1.1: Cross-section of a cathode ray tube (CRT) display and a field emission flat panel display (FEFPD). The diagram illustrates the extreme reduction in depth achieved by the FEFPD when compared to the CRT display.

Field emission can also be utilized to realize a variety of sensors. One example is a field emission vacuum gauge. The emitted electrons would ionize any gasses in the vacuum region. The ionized gases would result in an ion current that is proportional to the pressure in the vacuum. Hence, the ion current can be measured to make an indirect reading of the vacuum. This type of pressure gauge can be classified as an ionization vacuum gauge. Another type of gauge (which is used heavily) also classified as an ionization gauge, uses thermionic emission rather than field emission as its electron emission mechanism. Since thermionic emission is used, this gauge has a larger power

consumption than the field emission gauge. In addition, it suffers from out-gassing problems due to the high temperature requirement. The thermionic gauge is much larger than the field emission gauge would be, thus creating a waste of precious vacuum space. The field emission gauge has definite advantages over the thermionic emission gauge.

1.2 Field Emission Materials

Many different types of materials and structures have been used as field emitters. The most successful examples have relied on using emitter geometries with dimensions in the nanometer range to create very large, yet localized, electric fields at relatively low applied voltages. The typical geometry used is an array of cones. The cones have heights in the micrometer range and the radius of curvature at the cone apex is in the nanometer range. The arrays are typically termed field emitter arrays. Silicon and various types of metals including molybdenum [23], zirconium and hafnium [24], gold [25], platinum, and titanium [26] have been used to fabricate field emitter arrays, with each type of material possessing distinct advantages and disadvantages over the other.

1.2.1 Metals

The most common method used to fabricate metal arrays is the process developed by Spindt [14] [23]. A schematic outline of Spindt's process is given in figure 1.2. The process involves depositing a dielectric on a conductive substrate and then depositing a parting layer (usually aluminum) on the dielectric. An opening, which defines the location of a metal cone, is etched through the parting and the dielectric layer using standard photolithographic techniques. Evaporated metal is then deposited normal to the

surface to form a metal cone in the opening. Finally, the parting layer is removed to complete the metal field emitter array.

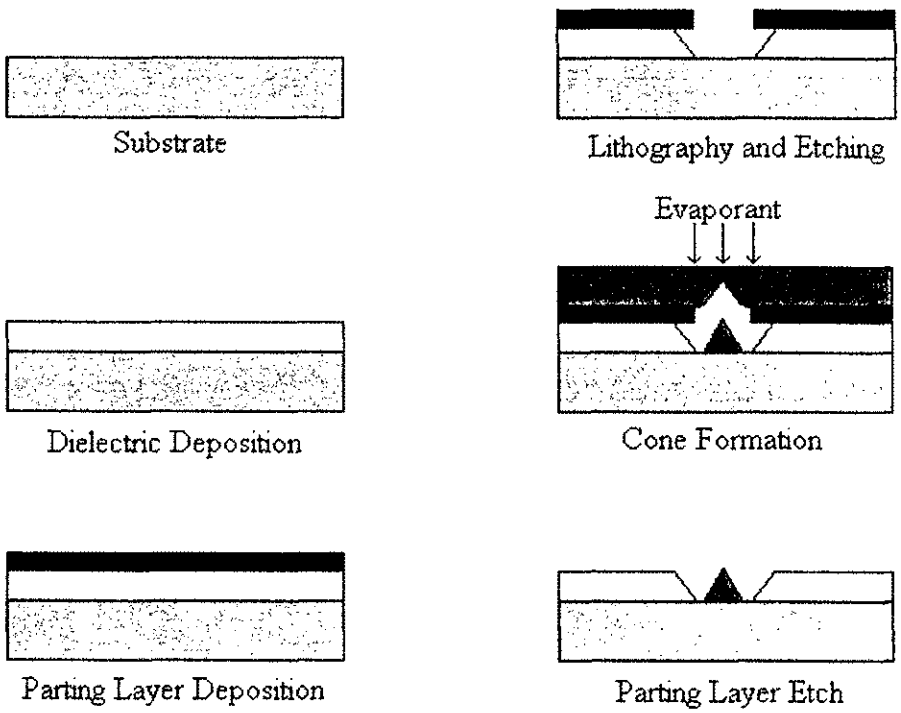


Figure1.2: Major fabrication steps involved in producing a metal field emitter array using the process developed by Spindt [14].

1.2.2 Silicon

In terms of fabrication simplicity, silicon arrays have the distinct advantage over metal arrays due to the ability to micromachine silicon. Fabrication of silicon field emitter arrays involves fewer fabrication steps and is less complicated than the metal process. In its simplest form, the silicon process has two main fabrication steps. First, an etch mask layer is deposited and patterned on a silicon substrate. The most common

masking layer is silicon dioxide, which requires only the inexpensive and simple process of growing a layer of silicon dioxide and patterning the silicon dioxide using standard photolithographic techniques. Second, anisotropic etching of silicon is used to create the silicon cones. Anisotropic etching is achieved either through wet chemical etching or dry etching. Of the two choices wet chemical etching is the cheapest and simplest; however, dry etching offers improved cone uniformity.

Another advantage of using silicon is that other devices such as control circuitry can be fully integrated onto the wafer with the silicon array. Circuit integration is not possible with metal arrays, creating the need for external control circuitry, hence increasing the overall size of the device.

1.3 Scope of the Research

For any type of field emitter array, geometric uniformity and reproducibility are critical factors that determine the ability to fabricate a group of arrays with identical field emission performance. To this end, the focus of this thesis is to present two very simple and inexpensive silicon field emitter array fabrication processes. The two processes will be compared in terms of the geometric uniformity and in terms the field emission performance of the resulting arrays. From these comparisons it will be determined which fabrication process produces the most geometrically uniform array and if the most uniform array does indeed produce the most consistent field emission.

Chapter 2 of this thesis provides the theoretical background of the silicon field emitters and the theory of field emission from silicon emitters. Chapter 3 describes the silicon field emitter array fabrication processes and the procedures used to measure their

geometric uniformity and field emission performance. The results of the study are presented in chapter 4 along with a detailed analysis and discussion. Finally, in chapter 5 conclusions on the performance of each fabrication process are presented.

CHAPTER II

THEORY

The fabrication and characterization of silicon field emitter arrays requires a detailed knowledge of silicon micro-machining and field emission processes. Therefore, the intent of this chapter is to present the theoretical aspects of these topics. Silicon micro-machining processes to be discussed are silicon oxidation and wet anisotropic silicon etching. For silicon oxidation the Deal-Grove equation, which describes the oxide thickness as a function of oxidation time, will be given. For wet silicon etching, the principle of etch anisotropy will be developed through a description of the crystal structure of silicon. In addition, various etchants will be given along with their etch characteristics, advantages, and disadvantages. Finally, the theory of field emission will be presented. The Fowler-Nordheim (F-N) equation, which relates the field emission current to the applied electric field and various material parameters, is given along with a method to fit experimental field emission data to the F-N equation.

2.1 Theory of Silicon Oxidation

The oxidation of silicon to produce a layer of silicon dioxide (SiO_2) on the silicon surface is an important process in the fabrication of silicon devices. Applications of silicon dioxide include its use as an insulator, masking layer, and passivation layer in VLSI device fabrication. In addition, silicon oxidation can be used in a silicon micro-machining process to remove very small amounts of silicon. This is possible since a

layer of silicon is consumed during the growth of a silicon dioxide layer. Silicon dioxide as a masking layer is also important in a micro-machining process. For these reasons, the theory of thermal oxidation of silicon is given below.

The chemical reactions describing the thermal oxidation of silicon in oxygen or water vapor are given by the following equations:

$$Si(solid) + O_2 \rightarrow SiO_2(solid)$$
$$Si(solid) + H_2O \rightarrow SiO_2(solid) + 2H_2$$

The reactions are termed dry and wet oxidation respectively.

As oxidation proceeds, the Si-SiO_2 interface moves into the silicon. Experiments have established that oxidation proceeds by the diffusion of the oxidizing species through the SiO_2 to the Si-SiO_2 interface where the oxidation reaction occurs [1].

The volume of SiO_2 is greater than the volume of silicon consumed as shown by the calculation below:

$$VolumeOfOneMolOfSi = \frac{MolecularWeightOfSi}{DensityOfSilicon} = \frac{28.09g/mol}{2.33g/cm^3} = 12.06\frac{cm^3}{mol}$$

Similarly, the volume of one mol of SiO_2 is calculated to be 27.18 cm^3/mol. Taking the ratio of the volume of one mol of silicon to the volume of one mol of SiO_2 yields

$$\frac{VolumeOfOneMolOfSi}{VolumeOfOneMolOfSiO_2} = \frac{12.06}{27.18} = 0.443 = \frac{Thickness * AreaOfSi}{Thickness * AreaOfSiO_2}$$

From this analysis, it is concluded that for SiO_2 of thickness d, a silicon layer of thickness 0.443d is consumed during the oxidation as shown by figure 2.1 [18].

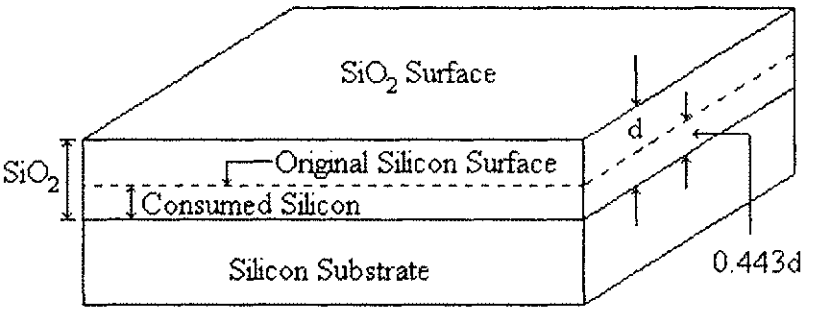


Figure 2.1: Silicon consumed during thermal oxidation [18].

The linear-parabolic model for silicon oxidation developed by Deal and Grove accurately predicts SiO_2 thickness as a function of growth time. The model is valid for temperatures between 700 and 1300°C, partial pressures between 0.2 and 1 atm, oxide thickness between 300 and 20,000Å, and for wet or dry oxidation. In addition, the model is only valid for predicting the oxide thickness on planar surfaces. The model was developed by considering the steady-state flux of oxidizing species from the gas phase, through the existing oxide layer to the Si-SiO_2 interface, and the reaction flux at the Si-SiO_2 interface. The result is the Deal-Grove equation given by [2]

$$d = \frac{A}{2}\left[1 + \frac{t+\tau}{A^2/4B}\right]^{1/2} - \frac{A}{2}$$

where

$$A = 2D\left[\frac{1}{k_s} + \frac{1}{h}\right]$$

$$B = \frac{2DC^*}{N_1}$$

$$\tau = \frac{d_i^2 + Ad_i}{B}$$

Here, D is the diffusion coefficient for the oxidizing species through the oxide, k_s is the rate constant of chemical surface reaction for silicon oxidation, h is the gas phase mass

transfer coefficient, C^* is the equilibrium bulk concentration of oxidizing species in the oxide, N_1 is the number of oxidant molecules in a unit volume of the oxide, and d_i is the initial oxide thickness.

Two interesting cases are for a short oxidation time (i.e. when $t + \tau << A^2/4B$) and for a long oxidation time (i.e. when $t + \tau >> A^2/4B$). For a short oxidation time, the Deal-Grove equation reduces to linear form

$$d = \frac{B}{A}(t + \tau) .$$

For a long oxidation time the Deal-Grove equation reduces to the parabolic form

$$d^2 = Bt .$$

These results indicate that the oxidation rate is initially *reaction limited*, but as the oxide layer becomes thicker the oxidation rate becomes *diffusion limited* [1].

In the experiments described in the later chapters of this thesis, silicon dioxide was grown using a tube style oxidation furnace. To determine the constants A and B in the Deal-Grove equation for the furnace used, measurements of oxide thickness as a function of growth time were made. The results are plotted in figure 2.2. Substituting the measured data points into the Deal-Grove equation and assuming $\tau = 0$, the constants A and B were determined to be:

$A = 0.1148\text{um}$

$B = 0.1642\text{um}^2/\text{h}.$

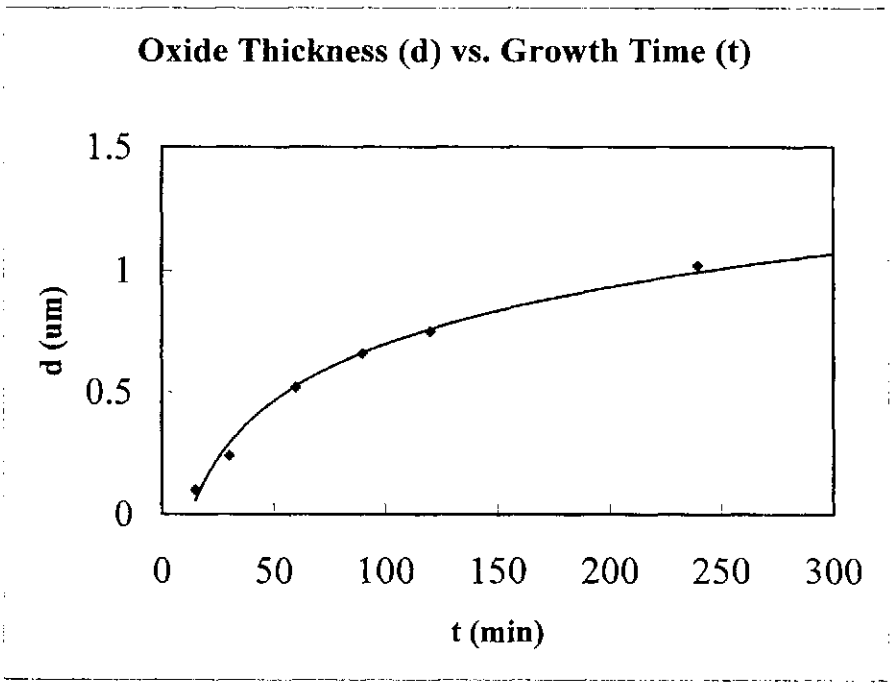


Figure 2.2: Experimentally measured oxide growth curve. Oxidation temperature was 1050°C.

In the case of non-planar silicon such as concave, convex, trenched, or ridged surfaces, the oxidation rate predicted by the Deal-Grove equation is invalid. Saraswat et. al. has shown that the oxidation rate is faster for convex surfaces and slower for concave surfaces when compared to the oxidation rate for planar surfaces [27].

2.2 Theory of Anisotropic Wet Etching

Anisotropic wet etching is used to fabricate a variety of three-dimensional silicon microstructures on single crystal silicon. Some examples include diaphragms and cantilevers for pressure and acceleration sensors or pyramid shaped tips for field emission applications. Here, the anisotropic wet etching of (100) oriented single crystal silicon is described. Some anisotropic wet etchants are given with special emphasis on potassium

hydroxide (KOH) and tetramethylammonium hydroxide (TMAH) in the form of chemical formulations, reactions, etch rates (as a function of temperature, concentration, and crystal orientation), degree of anisotropy, and the degree surface roughness.

2.2.1 Crystal Structure

Single crystal silicon is a covalently bonded solid in which four silicon-silicon bonds are arranged in a tetrahedral configuration as shown in Figure 2.3a. Each singly bonded silicon atom in this configuration will bond with four other silicon atoms to form an interconnected tetrahedral structure. This tetrahedral bonding scheme results in what is known as the diamond crystal structure. The unit cell, given in Figure 2.3b, is face-centered cubic and contains eight silicon atoms and has lattice parameter a = 5.431Å.

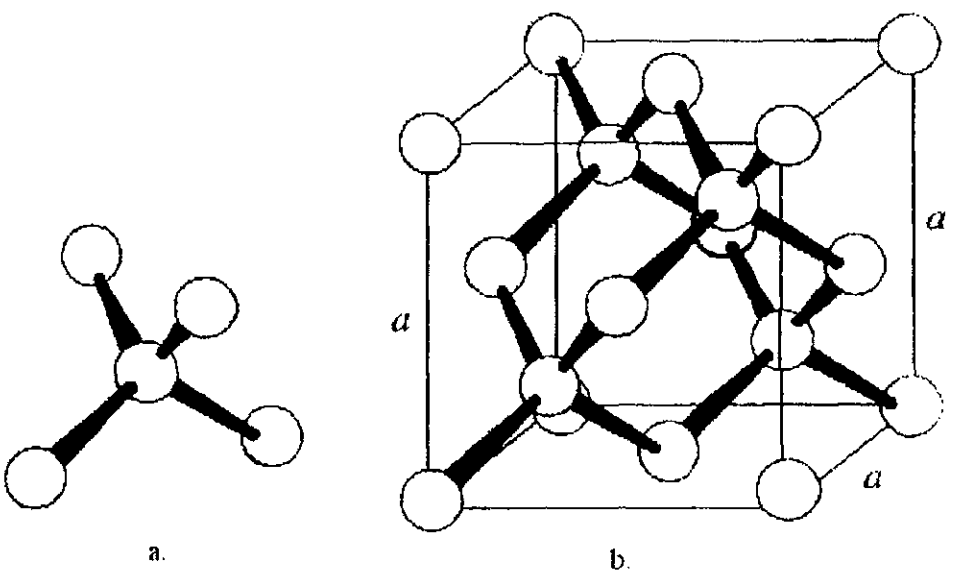


Figure 2.3: a. Tetrahedral bonding structure. b. Diamond crystal lattice unit cell.

Silicon is an anisotropic crystal, meaning certain crystal properties vary depending on the orientation of or direction into the crystal. Three important crystallographic directions for silicon are given in figure 2.4a and are denoted <100>, <110>, and <111>. Also important to the crystal properties are the various crystallographic planes found in the crystal. The three crystallographic planes corresponding to the above directions are shown in figure 2.4b and are denoted (100), (110), and (111). As can be seen from figure 2.4, the crystallographic direction is normal to its corresponding crystallographic plane.

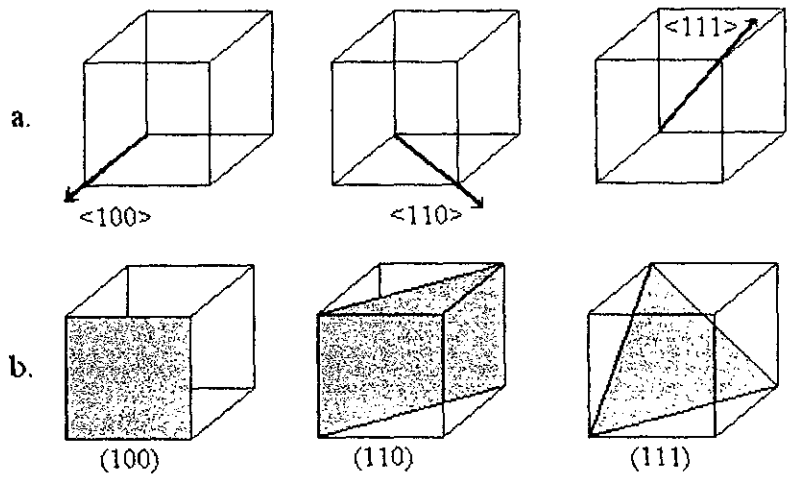


Figure 2.4: a. Three crystallographic directions for silicon superimposed on the unit cell. b. The corresponding crystallographic planes.

When the crystallographic planes given above are superimposed on the diamond crystal structure, as in figure 2.5, the number of atoms per unit area on each of the given crystallographic planes can be counted. From figure 2.5, it can be seen that there are 2 atoms on the (100) plane, 4 atoms on the (110) plane, and 2 atoms on the (111) plane. In terms of the lattice parameter 'a', the areas of the (100), (110), and (111) planes are a^2,

$\sqrt{2}a^2$, and $\left(\sqrt{3}/2\right)a^2$ respectively. From the above results, it is found that there are $2/a^2$ atoms/unit area on the (100) plane, $4/\sqrt{2}a^2$ atoms/unit area on the (110) plane, and $4/\sqrt{3}a^2$ atoms/unit area on the (111) plane. Therefore, it is concluded that the atomic packing density is highest on the (110) planes followed by the (111) and the (100) planes respectively.

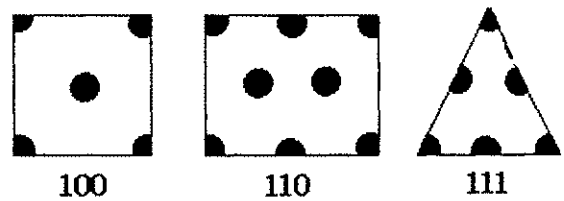


Figure 2.5: Illustration of the atoms that intersect the (100), (110), and the (111) crystallographic planes in the diamond crystal structure.

An important specification of a silicon wafer is the wafer's orientation. The orientation refers to how the crystallographic directions are arranged with respect to the surface of the wafer. For a <100> oriented silicon wafer, which is diagramed in figure 2.6, the <100> crystallographic direction is normal to the wafer surface, and the direction of the 'wafer flat' is parallel to the <110> crystallographic direction.

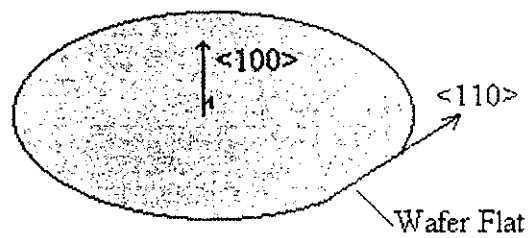


Figure 2.6: Schematic of a <100> oriented silicon wafer.

2.2.2 Wet Anisotropic Etching

Certain wet chemical silicon etchants are known to etch different crystallographic directions at different rates. In general, etching proceeds in the <110> direction the fastest, followed by the <100> direction, and finally, the <111> direction is etched the slowest. There is no accepted explanation for this phenomena, however several theories have been proposed. The most common of these is based on the combined effects of the variation of atomic packing density and bond strength with crystallographic plane. As discussed above, the atomic packing density is highest on the (111) plane followed by the (110) and the (100) planes. In addition, the silicon-silicon bond strength is thought to be larger on the (111) planes than that of the (100) and (110) planes.

Because of the etch anisotropy (i.e., the slow etch rate in the <111> crystallographic direction), the silicon (111) planes serve as effective 'etch stop' boundaries. The ability to stop on a given (111) plane depends on the orientation of the (111) planes with respect to the etching surface and on the pattern of the etch mask opening on the etching surface (an etch mask is any material on the etch surface that prevents etching). As an example, consider a <100> oriented silicon wafer with a rectangular etch mask opening as shown in figure 2.7. In figure 2.7a the etch mask opening is aligned to the <110> crystallographic direction, whereas in figure 2.7b the etch mask alignment is arbitrary. Figures 6c and d represent the terminal etch geometry for the etch masks of figures 6 a and b respectively. In each case the terminating etch surfaces are (111) silicon planes, which intersect to form an 'inverted rectangular pyramidal' hole. In the case where the etch mask was arbitrarily oriented, etch mask 'undercutting' occurred before the terminal (111) planes were reached. Therefore, the

etch mask opening serves only to define the maximum (111) plane exposure and hence the size of the pyramidal hole. It should be noted that before the terminal (111) planes are reached the geometry of the hole varies with etch time and is quite complex.

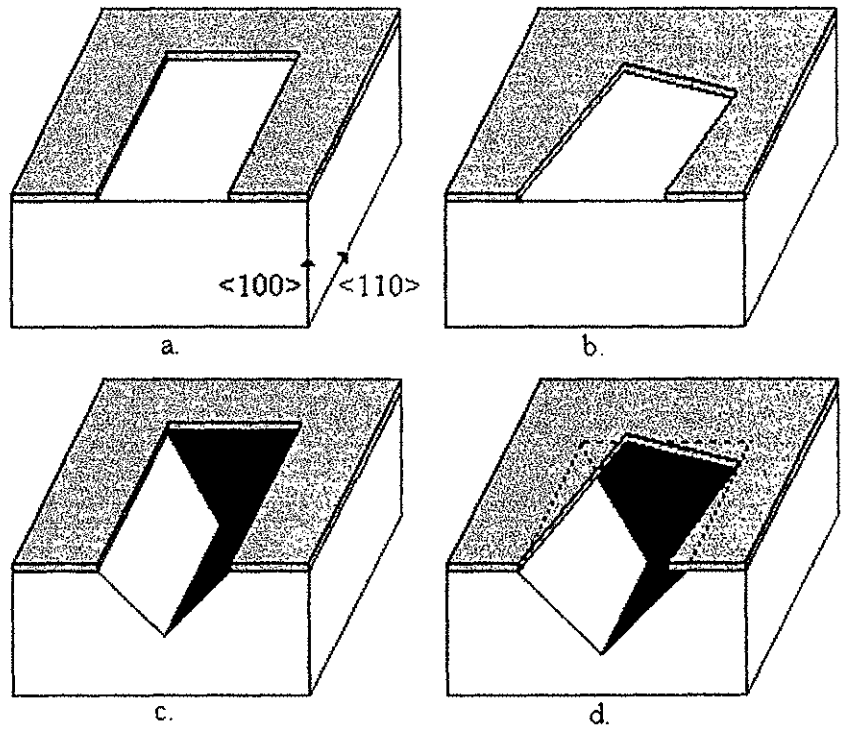


Figure 2.7: Cross-section through (100) silicon to demonstrate the effect of etch-mask alignment. a. Etch-mask aligned to <110> direction. b. Etch-mask arbitrarily aligned. c. Terminal etch geometry for aligned etch-mask. d. Terminal etch geometry for unaligned etch mask.

It is well known that the (111) planes intersect the (100) planes at an angle of θ=54.74° as shown in figure 2.8 [3]. Using this fact, the dimensions of the square pyramidal hole can be determined. The depth (d) of the hole is given by $d = \frac{W_{si} - W_h}{\sqrt{2}}$

where W_{si} and W_b are the length of the hole opening and hole bottom respectively. Note that in the limit as W_b tends to zero, the hole becomes the inverted pyramid. The amount of mask under-cut $U = W_{si}-W_{ox}$ is given by $U = \frac{R_{(111)}t}{\sin\theta}$ where $R_{(111)}$ is the etch rate of the (111) planes and t is the etch time. The amount of mask under-cut is generally quite small compared to the etch depth, due to the very slow etch rate of the (111) planes.

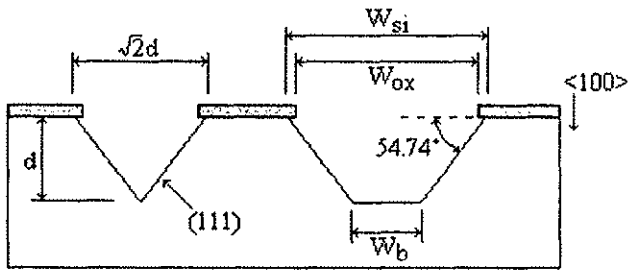


Figure 2.8: Dimensions of aniosotropically etched hole in (100) silicon [3].

Other etch mask patterns can be used to produce many etched geometries in silicon. An important consideration when using etch mask patterns other than the rectangular opening is convex corner undercutting. At convex corners, fast etching planes (such as (331), (311), (320), (210), (211), etc.) are exposed which etch relatively fast with respect to the (111) planes, hence a large amount of undercutting occurs at convex corners [4].

2.2.3 Etch Mask Materials

An etch mask is any material on the silicon surface that prevents silicon etching. Ideally, the etch selectivity of the silicon to etch mask would be infinite, that is the etch rate of the etch mask would be zero in whatever etchant is used. In practice this is not the

case, and in fact the etch rate of the etch mask depends on the etch mask material, type of etchant, etchant temperature, and etchant concentration.

The most common etch mask material is thermally grown silicon dioxide (SiO_2), due to its ease of growth, ability to be patterned using standard photolithographic techniques, and very low etch rate in most wet anisotropic etchants. Some other etch mask materials include deposited silicon dioxide, silicon nitride (Si_3N_4), and aluminum. Deposited silicon dioxide or silicon nitride might be used in the situation where the high temperature required for thermal silicon dioxide growth would damage the device under fabrication. Aluminum would possibly be used when aluminum is already serving some other function in the device and can 'double' as an etch mask. In general, the etch mask material chosen will depend on the exact details of the device fabrication. Specific information about the etch rates of some etch mask materials in various etchants will be given below.

2.2.4 Wet Anisotropic Etchants

There are several wet anisotropic silicon etchants. Each can be classified as belonging to one the following groups: alkali hydroxide, simple and quaternary ammonium hydroxides, or other. Several etchants belonging to the alkali hydroxide and simple and quaternary ammonium hydroxide groups will be given along with the corresponding chemical reactions, etch rates, and advantages/disadvantages of each. Etchants belonging to the 'other' group include EDP (a mixture of ethylenediamine, water, and pyrocatechol), hydrazine, and amine gallate compounds (a mixture of

ethanolamine, gallic acid, water, pyrazine, hydrogen peroxide, and a surficant). These etchants find little use and thus will not be discussed.

Alkali Hydroxide Etchants

The hydroxides of alkali metals such as KOH, NaOH, CsOH, and RbOH can be used to anisotropically etch silicon. Seidel *et al.* have proposed the following etch reaction [5] in which surface silicon atoms react with hydroxyl ions. This silicon is oxidized and four electrons are injected from each silicon atom into the conduction band

$$Si + 2OH^- \rightarrow Si(OH)_2^{2+} + 4e^- .$$

This causes the reduction of water, leading to the production of hydrogen

$$4H_2O + 4e^- \rightarrow 4OH^- + 2H_2 .$$

The silicon complex, $Si(OH)_2^{2+}$, further reacts with hydroxyl ions to form a soluble silicon complex and water

$$Si(OH)_2^{2+} + 4OH^- \rightarrow SiO_2(OH)_2^{2-} + 2H_2O \ .$$

Thus, the overall reaction is

$$Si + 2OH^- + 2H_2O \rightarrow SiO_2(OH)_2^{2-} + 2H_2 .$$

Note that the role of the alkali ions (K^+, Na^+, Cs^+, and Rb^+) can be neglected, since they do not appear in the reaction equations.

Factors controlling the etch rates of the various silicon planes are etchant concentration and temperature. The silicon etch rate in KOH first increases, then decreases with an increase in KOH concentration as shown in figure 2.9 [6]. In close agreement, Seidel found a maximum etch rate at 15%wt concentration using a KOH temperature of 72°C, [5]. He noted that concentrations below 15wt% produced an

insoluble white residue on the silicon surface. At concentrations below 30wt% the etched surface morphology is rough so, higher concentrations of 40-50wt% are typically used to minimize the surface roughness.

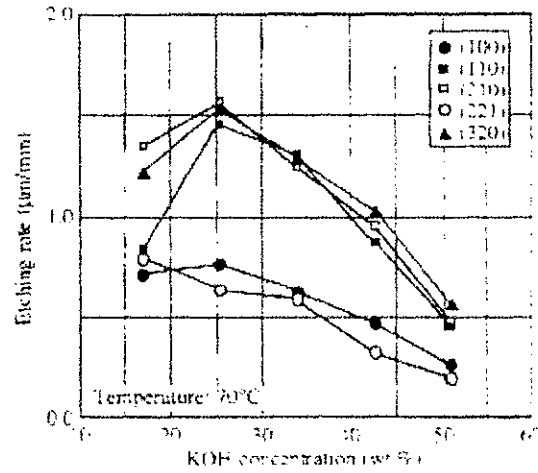


Figure 2.9: Silicon etch rate vs. KOH concentration for various crystal planes [6].

The silicon etch rate in KOH increases with an increase in KOH temperature as shown in figure 2.10 [6]. Of considerable interest for many applications of silicon anisotropic etching is the ratio of etch rates of the main crystallographic planes (i.e., the (100), (110), and (111) planes). The etch ratio of <110>:<100>:<111> in KOH was found to vary from 50:30:1 at 100°C to 160:100:1 at room temperature [5]. Hence, the anisotropy of KOH increases with a decrease in etch temperature.

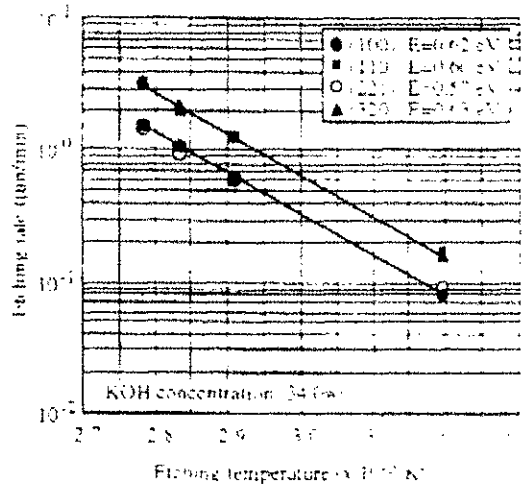


Figure 2.10: Silicon etch rate vs. KOH temperature for various crystal planes [6].

Two common etch mask materials used with the alkali hydroxide etchants are thermally grown silicon dioxide and CVD silicon nitride. The etch rate of silicon nitride in KOH as reported by Seidel *et al.* was zero [5]. For silicon dioxide, the etch rate was measurable and shown to increase with KOH temperature and concentration as given in figure 2.11 [5].

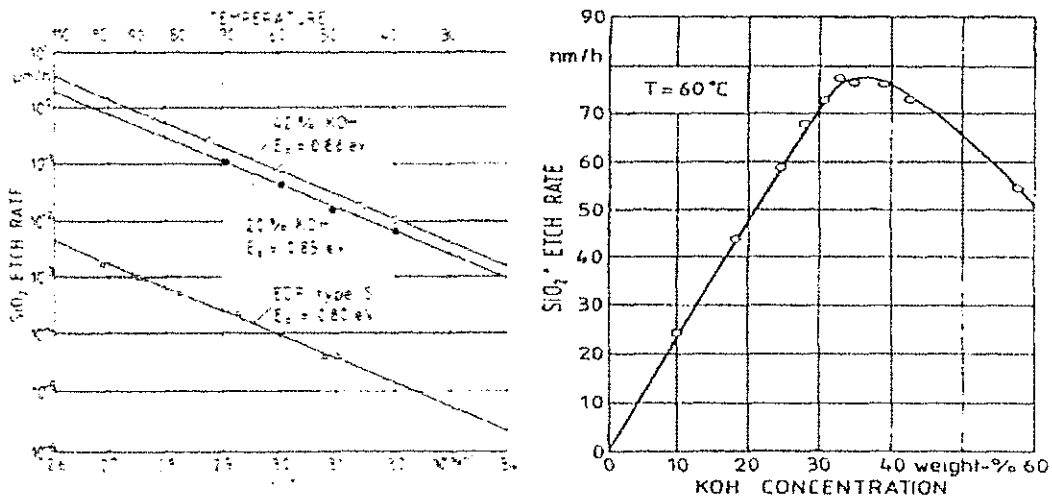


Figure 2.11: Silicon dioxide etch rate in KOH vs. KOH temperature and concentration [5].

A major disadvantage of the alkali hydroxide etchants are the alkali ions present in the etch solution. Alkali ions, especially sodium, can be detrimental to MOS devices. Hence, when fully integrated silicon devices (such as micro-machined pressure transducers with 'built-in' electronics) are to be fabricated, the use of alkali hydroxide etchants is probably not the best choice.

Simple and Quaternary Ammonium Hydroxide Etchants

To eliminate the alkali contamination problems associated with the alkali hydroxide etchants discussed above, the alkali-free simple and quaternary ammonium hydroxide etchants can be used. Two such ammonia-based etchants are ammonium hydroxide (NH_4OH) and the quaternary compound tetramethylammonium hydroxide (TMAH) ($(CH_3)_4NOH$). Little attention has been given to ammonium hydroxide, so the remainder of this section will focus on the properties of TMAH.

In a study by Michaud *et al.*, the silicon etching process in TMAH was characterized using Raman spectral analysis [7]. The main results of this study show that the final etch products are silicate ($SiO_2(OH)_2^{2-}$) and its polymers and that the concentration of OH^- ions is reduced during etching. These results suggest that the dissolution process in TMAH is the same as in KOH. Therefore, the net overall reaction for KOH etching can be adopted for TMAH etching.

Like KOH, the etch rate of silicon in TMAH depends on temperature and concentration. The etch rate increases with an increase in TMAH temperature as shown in figure 2.12 [6]. Figure 2.13 shows the etch rate dependence on TMAH concentration for various crystallographic planes [6]. Low TMAH concentrations tend to cause the formation of hillocks on the etched silicon surface; hence, concentrations above 20% are generally used.

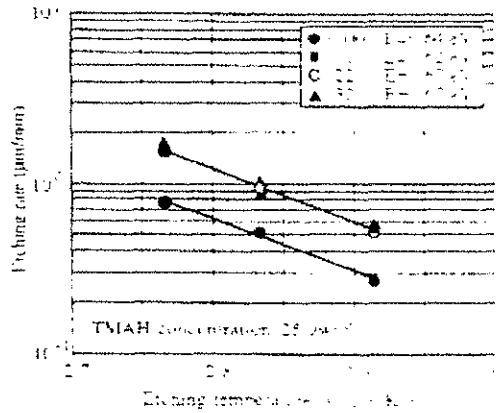


Figure 2.12: Silicon etch rate vs. TMAH temp for various crystallographic planes [6].

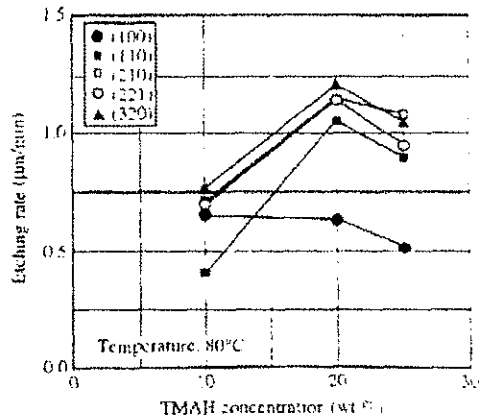


Figure 2.13: Silicon etch rate vs. TMAH concentration for various crystallographic planes [6].

A useful property of TMAH is the very low etch rate of silicon dioxide etch mask. Figure 2.14 gives the etch rate of wet and dry thermal silicon dioxide for two TMAH concentrations [8]. The etch rate of silicon nitride in TMAH is similar. A disadvantage is that TMAH etches aluminum quite readily. Various authors have shown that lowering the pH of TMAH decreases the etch rate of aluminum, but the lower pH also tends to reduce the anisotropy of the silicon etch as well as increasing the surface roughness [9].

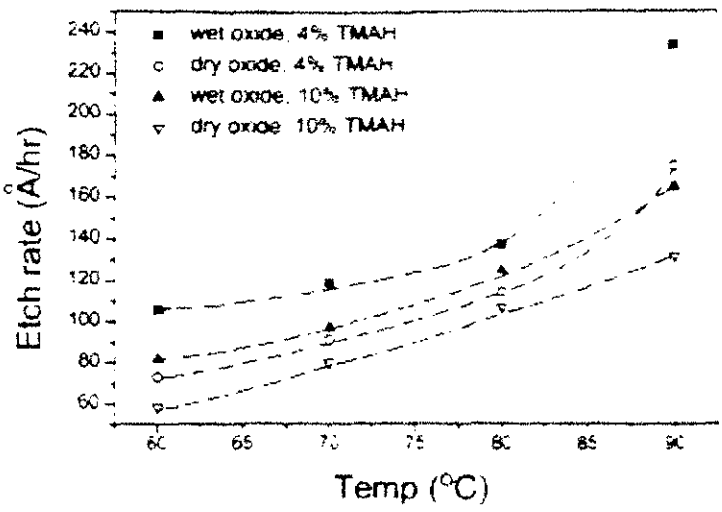


Figure 2.14: Etch rate of silicon dioxide vs. TMAH temperature [8].

Comparison of KOH and TMAH

From the above data concerning the etch rate of silicon in KOH and TMAH, it is concluded that the etch rate change as a function of temperature and concentration follow the same trend for both etchant types, and that the etch rates are relatively equal for both etchants. Both etchants have a very low silicon nitride etch rate, whereas the etch rate of silicon dioxide is high for KOH (10-700 nm/hour) but low for TMAH (10-20 nm/hour).

As mentioned above, an important consideration for applications of silicon anisotropic etching is the degree of anisotropy achieved, specifically the ratio of etch rates of various crystallographic planes. For both KOH and TMAH, these ratios will vary with temperature and concentration. In general, a higher degree of anisotropy is achieved with KOH than is with TMAH as illustrated in figure 2.15 [6].

Orientation	KOH (34.0wt.%, 70.9°C)			TMAH (20.0wt.%, 79.3°C)		
	Etching rate (μm/min)	Etching rate ratio		Etching rate (μm/min)	Etching rate ratio	
		(to <100>)	(to <111>)		(to <100>)	(to <111>)
100	0.629	1.000	74	0.603	1.000	57
110	1.292	2.054	151	1.114	1.847	65
210	1.237	1.967	145	1.154	1.914	72
211	0.983	1.563	115	1.132	1.877	69
221	0.580	0.922	69	1.142	1.894	69
310	1.079	1.715	126	1.164	1.964	72
311	1.065	1.693	125	1.225	2.028	74
320	1.285	2.043	151	1.211	2.008	73
331	0.845	1.343	99	1.099	1.822	67
530	1.273	2.024	149	1.097	1.819	66
540	1.283	2.040	150	1.135	1.882	69
111 *1	0.009	0.014	1	0.027	0.027	1

*1: Etching rate of (111) plane was separately measured using fan-shaped patterns as mentioned in the text.

Figure 2.15: Anisotropy comparison between KOH and TMAH [6].

The degree of surface roughness is a function of etchant concentration for KOH and TMAH. As the concentration is increased, the surface roughness decreases. This trend is illustrated if figure 2.16 [10]. Also evident from this figure is the fact that the surface roughness is always larger for TMAH etched surfaces than for KOH etched surfaces.

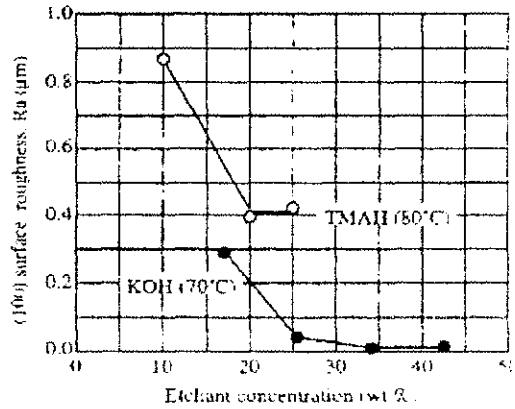


Figure 2.16: Surface roughness vs. etchant concentration for KOH and TMAH [10].

2.3 Theory of Field Emission

The emission of electrons from the surface of a material can occur as a result of any of four processes. These processes are thermionic emission, Schottkey emission, photo emission, and field emission. In thermionic, Schottkey, and photo emissions it is required that the electrons gain kinetic energy sufficient to overcome the potential energy barrier at the material surface. Field emission is fundamentally different from these emission processes in that instead of gaining kinetic energy to overcome the potential barrier, the electron tunnels through the potential barrier with finite probability. Hence, field emission is a quantum mechanical process.

Below, an analysis of field emission is presented. The analysis is based on field emission from metals, but is also valid for n-type semiconductors. This is true for the following reasons [11]. In an n-type semiconductor the Fermi energy level is close to the conduction band. Under the application of a large electric field, the conduction band at the surface will dip below the Fermi level. This results in a "pool" of electrons collecting at the surface. These electrons obey Fermi statistics; hence, n-type semiconductors can be treated as a metal under the application of a large electric field. Since the analysis for metals and n-type semiconductors can be treated the same, the word *material*, which implies metal or n-type semiconductor, will be used below.

2.3.1 Tunneling Phenomena

The potential barrier seen by an electron at a materials surface is given by the sum of the image potential energy and the potential energy due to an applied electric field [12]. The image potential energy is the potential energy of an electron just outside the

surface of the material and is due to the positive charge left in the material. Defining the potential energy of the electron to be zero in the material, letting x = 0 correspond to the surface of the material, and x > 0 correspond to being outside the material, the image potential energy as found using the theorem of image charges in electrostatics is given by

$$PE_{image}(x) = (E_f + \Phi) - \frac{e^2}{16\pi\varepsilon_0 x} \quad x > 0$$

where ε_0 is the absolute permittivity, e is the electronic charge, E_f is the Fermi energy, and Φ is the work function of the material. The potential energy due to the applied electric field F is given by

$$PE_{applied}(x) = -exF \quad x > 0.$$

The overall potential energy barrier seen by an electron is therefore

$$PE(x) = (E_f + \Phi) - \frac{e^2}{16\pi\varepsilon_0 x} - exF \quad x > 0.$$

This is shown graphically in figure 2.17. The applied electric field serves to decrease the height and width of the potential energy barrier. Specifically, the work function is reduced to an effective value given by

$$\Phi_{eff} = \Phi - \left[\frac{e^3 F}{4\pi\varepsilon_o}\right]^{1/2}$$

which was determined by finding the maximum of PE(x).

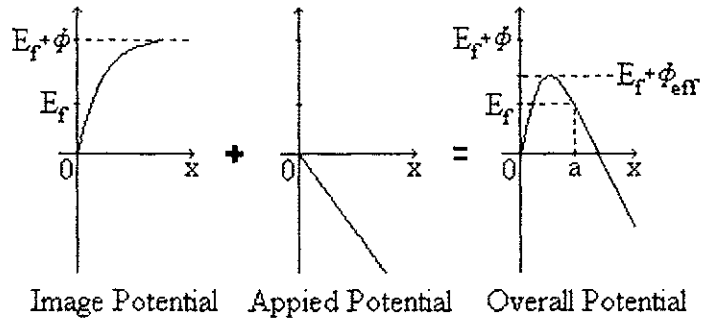


Figure 2.17: Potential energy "seen" by an electron at the surface of a material is the sum of the mage potential and the applied potential.

Approximating the potential barrier to be rectangular with height $V_o = E_f+\Phi_{eff}$ and width a as given in figure 2.18, the probability that an electron will tunnel through the barrier can be calculated from the one dimensional time independent Schrodinger equation which is

$$\frac{d^2\Psi}{dx^2}+\frac{8\pi^2 m}{h^2}(E-V)\Psi=0$$

where m is the effective mass of the electron, h is Plank's constant, E is the energy of the electron, and V is the potential energy seen by the electron. Dividing the electron's space into regions I, II, and III as shown in figure 2.18 the Schrodinger equation can be solved for each region resulting in three wave functions $\Psi_I(x)$, $\Psi_{II}(x)$, and $\Psi_{III}(x)$. Since the potential energy in regions I and III is zero the electron energy must be purely kinetic therefore, $\Psi(x)$ must be traveling waves. In region II, the kinetic energy of the electron is less than the potential barrier height V_o, which implies the wave function, should decay in this region.

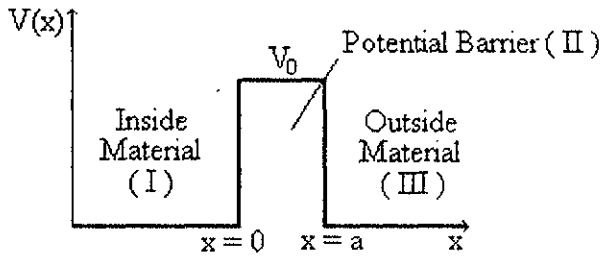


Figure 2.18: Rectangular potential energy barrier approximation.

The solutions to the one dimensional time independent Schrodinger equation subject to the conditions above are [12]

$$\begin{aligned} \Psi_I(x) &= A_1 \exp(jkx) + A_2 \exp(-jkx) && x < 0 \\ \Psi_{II}(x) &= B \exp(-\alpha x) && x \le 0 \le a \\ \Psi_{III}(x) &= C \exp(jkx) && x > a \end{aligned}$$

where

$$k = \sqrt{\frac{8\pi^2 mE}{h^2}}$$

and

$$\alpha = \sqrt{\frac{8\pi^2 (V_0 - E)}{h^2}}.$$

Here, $\Psi_I(x)$ represents the wave incident on the potential barrier where A_1 is the amplitude of the incident wave and A_2 is the amplitude of the reflected wave. $\Psi_{II}(x)$ represents an attenuating wave in the potential barrier with amplitude B, and $\Psi_{III}(x)$ represents the wave transmitted through the potential barrier with amplitude C.

The probability P that an electron will tunnel through the potential barrier is given by [12]

$$P = \frac{|\Psi_{III}(x)|^2}{|\Psi_I(x)_{incident}|^2} = \left[\frac{C}{A_1}\right]^2 .$$

Using the boundary conditions that $\Psi(x)$ and $\frac{d\Psi(x)}{dx}$ are continuous at x = 0 and x = a, the coefficients C and A_1 can be determined and used to calculate P. It turns out that P is given approximately by [12]

$$P \cong \exp\left[\frac{-4\pi(2m\Phi_{eff})^{1/2}a}{h}\right].$$

It can be seen that the probability for tunneling increases dramatically with a decrease in the barrier height and width. The barrier height and width decrease with an increase in the applied electric field F. Therefore, the probability increases with the applied electric field.

2.3.2 Fowler-Nordheim Relation

Fowler and Nordheim followed a similar but much more rigorous analysis to determine the tunneling probability. Multiplying this probability with the number of electrons arriving at the potential barrier, given for metals (and n-type semiconductors under application of large electric field) by the Fermi-Dirac distribution function, and integrating over the electron energy E, the total number of electrons tunneling through the barrier and the corresponding tunnel current can be calculated. The result is the Fowler-Nordheim (F-N) equation for field emission. The F-N equation relates the tunnel current density J to the applied electric field (F) and the material's work function (ϕ) and is [13]

$$J = \frac{e}{2\pi h}\frac{E_f^{1/2}}{(\phi + E_f)\phi^{1/2}} F^2 \exp\left[-\frac{4}{3}\left(\frac{8\pi^2 m}{h^2}\right)^{1/2}\frac{\phi^{3/2}}{eF}\right]$$

$$= 6.2x10^{-6}\frac{E_f^{1/2}}{(\phi + E_f)\phi^{1/2}} F^2 \exp\left[-6.8x10^7\frac{\phi^{3/2}}{F}\right]$$

where J is in amps/cm^2, F in volts/cm, and E_f and ϕ in eV.

The analysis by Fowler and Nordheim above was for a triangular potential barrier. The true barrier shape (as shown above in figure 2.17) has a rounded top due to the applied electric field. Accounting for this correction leads to the more accepted form of the F-N equation given as [14]

$$J = \frac{AF^2}{\phi t^2(y)}\exp\left(-B\frac{\phi^{3/2}}{F}v(y)\right)$$

where

$$A = 1.54x10^{-6},$$

$$B = 6.87x10^7,$$

and y is the Schottky lowering of the work function barrier given by

$$y = \frac{3.79x10^{-4}F^{1/2}}{\phi}.$$

The functions t(y) and v(y) are image correction factor functions that account for the rounding of the potential barrier due to the image charge effect. The functions have been evaluated and shown to be slowly varying functions of the applied field F. Therefore, t(y) and v(y) are generally approximated as

$$t^2(y) = 1.1$$
$$v(y) = 0.95 - y^2$$

over the operating range of most cathodes [14].

2.3.3 Correlation Between Theory and Experiment

Experimental observations of field emission are generally made by measuring the field emission current I as a function of the applied voltage V. Therefore, the substitutions

$$J = \frac{I}{\alpha}$$

and

$$F = \beta V$$

are made in the field emission equation where α is the emitting area and β is the field enhancement factor at the emitting surface in units of inverse length. Making the substitutions for J, F, t(y), and v(y) and simplifying yields

$$I = aV^2 \exp\left(\frac{-b}{V}\right)$$

where

$$a = \frac{\alpha A \beta^2}{1.1\phi} \exp\left(\frac{B(1.44x10^{-7})}{\phi^{1/2}}\right)$$

$$b = \frac{0.95B\phi^{3/2}}{\beta}.$$

Taking the natural logarithm of the simplified equation for field emission and rearranging yields

$$\ln\left(\frac{I}{V^2}\right) = -b\left(\frac{1}{V}\right) + \ln(a).$$

So, using experimentally determined I-V data, a plot of $\ln(I/V^2)$ vs. 1/V will yield a straight line with slope –b and intercept of ln(a) if the measured current is indeed due to field emission. From this plot, the constants a and b can be determined. In addition, if

the work function of the emitting material is known, the field enhancement factor and the emitting area can be determined using the equations

$$\beta = \frac{0.95B\phi^{3/2}}{b}$$

and

$$\alpha = \frac{1.1a\phi}{A\beta^2}\exp\left(-\frac{B(1.44x10^{-7})}{\phi^{1/2}}\right).$$

2.3.3.1 The Field Enhancement Factor (β)

An electric field of roughly $4x10^7$ volts/cm is required for field emission [17]. Consider two flat parallel plate electrodes separated by a distance d. The application of a voltage V across the plates creates a uniform electric field E between the plates given by

$$E = \frac{V}{d}.$$

If a distance of 1 micron separated the electrodes, 4kV of voltage would be required to produce the electric field required for field emission.

As the geometry of the electrodes deviates from the flat parallel case, the electric field is no longer uniform over the area of the plates. The true electric field is now a function of the position on the plates. The effective electric field F given by

$$F = \beta V$$

removes the position dependence of the field by introducing the field enhancement factor β. The effective field is a constant, and is analogous to the average value of the true electric field.

The field enhancement factor is a constant with units of inverse length and is a function of the geometry of the electrodes. Using experimental data and numerical simulation methods, it has been shown that electrodes with cusp-shaped cones (an example is shown in figure 2.19) on the surface will have the largest field enhancement factor [15]. In addition, it has been shown that the field enhancement factor will increase with a decrease in the cone radius [15] [16]. Using the cusp-shaped cone geometry, field emission has been observed at voltages of less than 100V.

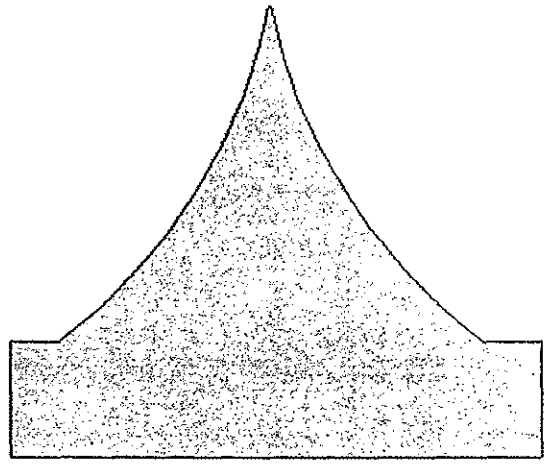


Figure 2.19: Schematic of a cusp-shaped silicon nano-tip.

Analytic evaluation of the field enhancement factor for cone shaped emitters by Kosmahl, has shown that the field enhancement factor is directly proportional to the cone height and inversely proportional to the cone radius [22]. Specifically, the relation

$$\beta \propto \frac{2h/r}{\ln(4h/r)-2}$$

where h is the height of the cone, and r is the radius of curvature at the apex of the cone was derived. This relation is significant because it describes the relationship between

conical electrode dimensions and the field enhancement factor. Hence, field emission is a function of the electrode geometry.

CHAPTER III

EXPERIMENTS

The field emission current from the surface of a material is dependant on the applied voltage (V), the work function of the material (ϕ), the emission area (α), and the field enhancement factor (β) as described by the Fowler-Nordheim (F-N) relation. The field enhancement factor relates the voltage applied to field emitter to the effective electric field at the material surface and is a function of the geometry of the emitter surface. Therefore, in order to produce field emitters with identical performance, the geometry of the emitters must be controlled by fabrication methods.

One type of field emitter is a silicon field emitter array. This is simply an array of cusp-shaped silicon cones micro-machined on the surface of silicon whose radius of curvature at the cone apex is in the nanometer range. The cusp-shaped geometry is used to realize a high field enhancement factor so that field emission can be achieved at relatively low applied voltages. In the following sections details of two field emitter array fabrication processes and an experiment designed to compare the two processes will be given.

3.1 Field Emitter Array Fabrication

All field emitter arrays were fabricated using (100) oriented n-type silicon (antimony doped) with 0.005-0.020 Ω-cm resistivity. Low resistivity n-type silicon was

used to maximize the transport of electrons from the bulk material to the surface. The silicon field emitter array fabrication process involved thermal silicon oxidation, photolithography, and wet anisotropic silicon etching.

The two field emitter array fabrication processes, termed the standard fabrication process and the new fabrication process are based on these techniques. The standard field emitter fabrication process is widely used, details of which are given below and can also be found elsewhere in literature [21]. The new field emitter array fabrication process is based on the standard process, with some modifications. The intent of the modifications is to improve the uniformity of the field emitter array, and hence improve its field emission performance and consistency.

3.1.1 Standard Field Emitter Array Fabrication Process

The standard fabrication process involves three main process steps, which are oxide patterning, wet anisotropic silicon etching, and oxidation sharpening. Each main step is described in detail in the following three sections.

3.1.1.1 Oxide Patterning

The outcome of this process step is an array of silicon dioxide squares patterned on the surface of a silicon sample. Each oxide square defines the location of a single silicon nano-tip. The oxide squares are approximately 0.3um thick, 10um on a side, and spaced 10um apart in all directions as shown in figure 3.1. One side of the squares is aligned parallel to the (110) direction of the silicon sample. The array size is 20x20, resulting in 400 oxide squares, and therefore 400 nano-tips.

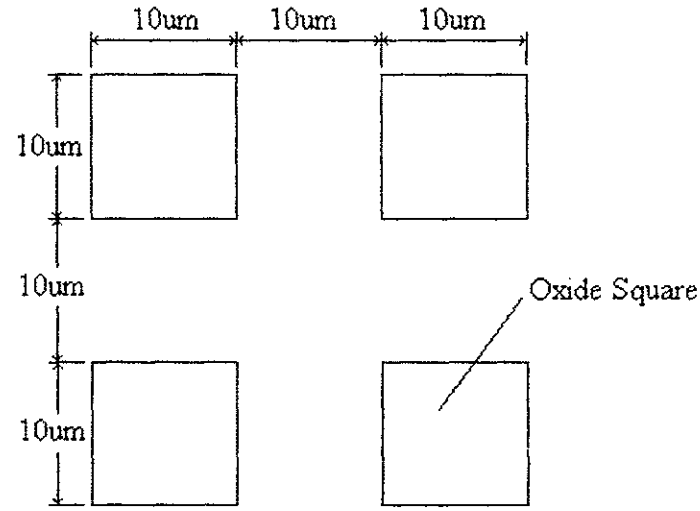


Figure 3.1: Schematic of a portion of the patterned oxide.

The process begins by cleaning the silicon in a hot (≈120°C) ultrasonically agitated sulfuric acid bath followed by a rinse in deionized water. Next, a 0.3um layer of oxide is grown on the silicon using a wet thermal oxidation process. The oxidation is performed in a tube style oxidation furnace at 1050°C in an ambient of nitrogen and water vapor at atmospheric pressure. Total oxidation time is 30 minutes.

Photolithography is used to pattern the oxide layer. A thin layer of photo-resist, approximately 1um, is spin coated on the oxide layer and baked to dry. The photo-resist coated sample is then aligned to a photo-mask. The photo-mask is a high contrast pattern that is an identical representation of the desired oxide pattern (i.e., the photo-mask is opaque to ultra-violet light at the locations of the oxide squares, and transparent everywhere else). The silicon is aligned to the photo-mask when one edge of the squares is parallel to the silicon's (110) crystallographic direction. This alignment is necessary since the oxide squares are to be used as etch masks during the aniosotropic silicon etch

step. Different alignments will produce nano-tips with different shapes. After alignment, the photo-mask is brought in contact with the photo-resist, followed by exposure to ultra-violet light for 4.5 minutes. Next, the exposed sample is developed in a liquid developer solution. The developer removes the regions of photo-resist exposed to ultra-violet light, whereas the regions of photo-resist not exposed to ultra-violet light remain. The result is a pattern of photo-resist squares on the oxide layer.

Finally, the photo-resist squares are used as an etch mask during chemical etching of the oxide layer (i.e., the oxide will not be etched at the locations of the photo-resist squares.) The oxide layer is chemically etched by immersing the sample in 49% buffered hydrofluoric acid (BHF). The etch rate of the oxide in BHF is approximately 1000 Å/minute. Therefore, an etch time of 3 minutes was used to completely remove the oxide. After oxide etching, the remaining photo-resist is removed using acetone, leaving behind the patterned oxide squares on the silicon surface.

3.1.1.2 Wet Anisotropic Silicon Etching

The result of this process step is a pyramid shaped tip at the location of each oxide square. The pyramid shaped tips are created using wet anisotropic silicon etching. The etchant used is tetra methyl ammonium hydroxide (TMAH). Another possible etchant is potassium hydroxide (KOH). TMAH was chosen over KOH due to its low silicon dioxide etch rate and CMOS compatibility.

To form the pyramid shaped tips, the patterned oxide silicon sample is first cleaned in hot sulfuric acid and rinsed as described above. The sample is then dipped in dilute BHF (2.5%) for 5 seconds to remove any natural oxide from the silicon surface.

This is necessary since an oxide layer will prevent silicon etching. Next, anisotropic silicon etching is performed by immersing the sample in TMAH. The etch rate and etch anisotropy of silicon in TMAH is a function of TMAH temperature, concentration, and pH. Therefore, the TMAH temperature and concentration were held at 80±2°C and 40±2% respectively. The silicon etch rate at this temperature is slow enough to allow good control of the etching, but fast enough so that the etching is complete in less than 10 minutes. This TMAH concentration was chosen since concentrations below 25% result in a rough silicon surface. Dissolved silicon affects the pH of TMAH, so new TMAH was used to etch each sample.

The samples were etched in one-minute increments by removing them from the TMAH and quenching in deionized water. It was found that the uniformity of the tips is better using this technique, rather than etching in longer time intervals. After each one-minute etch interval the sample was inspected under an optical microscope to monitor the etch progress. When etching begins, TMAH begins to dissolve all silicon not masked by silicon dioxide. Soon after etching starts, under cutting of the oxide squares begins. As etching proceeds, more silicon is removed in the (100) crystallographic direction than in other directions due to the anisotropy of TMAH. Etch progress is monitored by observing the amount of under cutting of the oxide squares. Near the end of the etch cycle, the oxide squares are very close to being removed from the silicon sample due to the large amount of silicon under cutting. At this point, the length of the etch time interval is reduced, so that etching will stop as soon as the oxide squares are removed. The pyramid tips are fully etched the instant the oxide squares are removed from the nano-tips. A schematic of the etch progress in the form of a cross-section and a top view

is given for a single tip in figure 3.2. The top view is a representation of what is seen when monitoring the etch progress under an optical microscope. Since the oxide square is transparent, the width of the silicon connecting the oxide square to the nano-tip can be seen.

This field emitter array fabrication process can be considered a "low-uniformity" process because it is difficult to determine exactly when the oxide squares are removed due to the extremely small size. In addition, not all oxide squares are removed at the same time due to variation in oxide mask sizes and temperature and concentration gradients within the TMAH etchant. For these reasons, it is very likely that some of the tips in the array will be 'over-etched.' An over-etched tip is one that is etched after the oxide mask has been removed. Over-etching results in a quick reduction in tip height and sharpness. Hence, this process is likely to produce an array of nano-tips with large variation in tip height and sharpness.

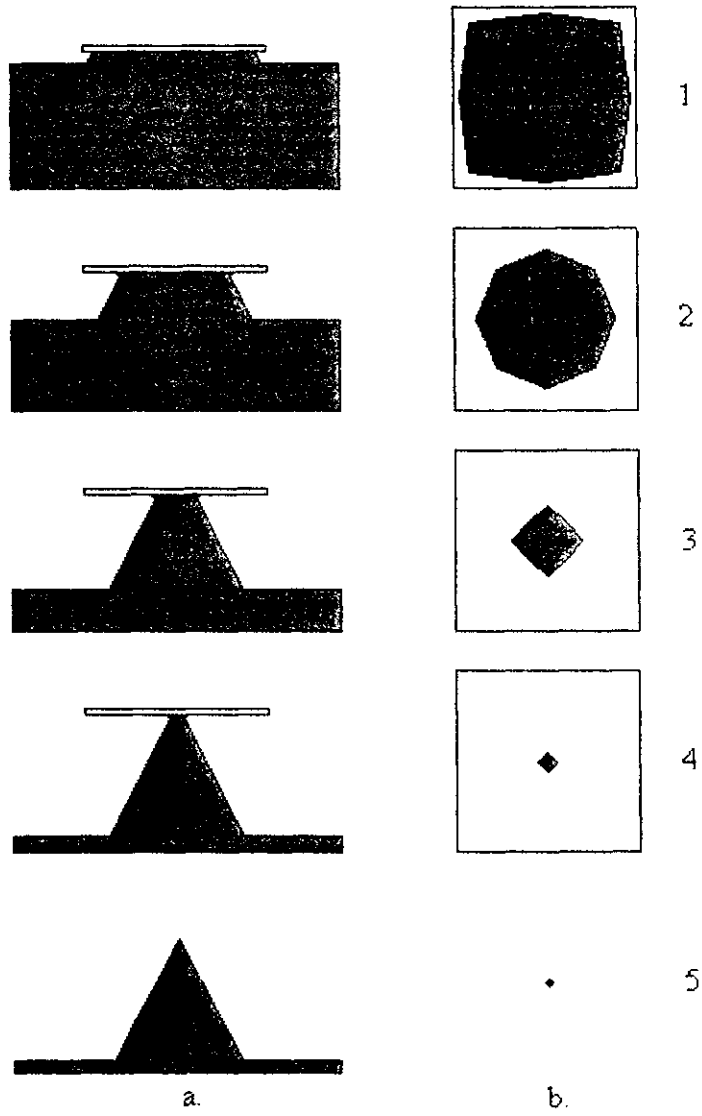


Figure 3.2: Schematic representation of the etch progress for a single pyramid tip. Column a. is a cross-section, and column b. is a top view of the tip as seen under an optical microscope. Row 1 represents the tip just after etching begins, and row 5 represents the completely etched tip.

3.1.1.3 Oxidation Sharpening

Oxidation sharpening serves to increase the nano-tip sharpness and change the overall tip geometry from pyramidal to a cusp shape; hence, the field enhancement factor of the field emitter array is increased. Oxidation sharpening is a process in which the silicon field emitter array is thermally oxidized and the resulting oxide layer removed.

This process step begins by cleaning the array in hot sulfuric acid and rinsing in deionized water. Next, the array is oxidized using wet thermal oxidation. It has been shown that a one-hour oxidation at 1050°C, which results in an oxide thickness of 0.4um, will maximize the nano-tip sharpness without reducing the tip height appreciably [16]. To complete the oxidation sharpening step and the entire standard field emitter array fabrication process, all the oxide is chemically removed from the array using BHF.

3.1.2 New Field emitter Array Fabrication Process

The new fabrication process also involves three main process steps, which are oxide patterning, wet anisotropic silicon etching, and oxidation sharpening. This process differs from the standard process in the wet anisotropic silicon etch step. The details of this process step and the others are described in the following three sections.

3.1.2.1 Oxide Patterning

This process step is identical to the oxide patterning step for the standard field emitter array fabrication process (section 3.2.1.1). Skipping the processing details, the result of oxide patterning is a 20x20 array of 0.3um thick silicon dioxide squares on a silicon sample. The oxide squares are 10um on a side and are spaced 10um in each direction. One side of the squares is aligned parallel to the (110) crystallographic direction of the silicon sample.

3.1.2.2 Wet Anisotropic Silicon Etching

Again, this process step is nearly identical to the wet anisotropic silicon etch step for the standard process (section 3.2.1.2). TMAH is used to anisotropically etch silicon resulting in pyramid-shaped tips at the location of each oxide square. TMAH temperature and concentration are 80±2°C and 40±2% respectively. The main difference here is that silicon etching is stopped just before the oxide squares are removed as shown in figure 3.3. The result is a pyramid shaped tip topped with the oxide square and is termed "oxide on" tip. The silicon neck connecting the tip to oxide square is approximately 0.5um.

Since the oxide squares are not removed from the silicon tips during silicon etching, etching of the top of the tips is prevented. Hence all the "oxide on" tips are the same height. For this reason, the new fabrication process by design should produce field emitter arrays with better uniformity and field emission performance than arrays produced by the standard process.

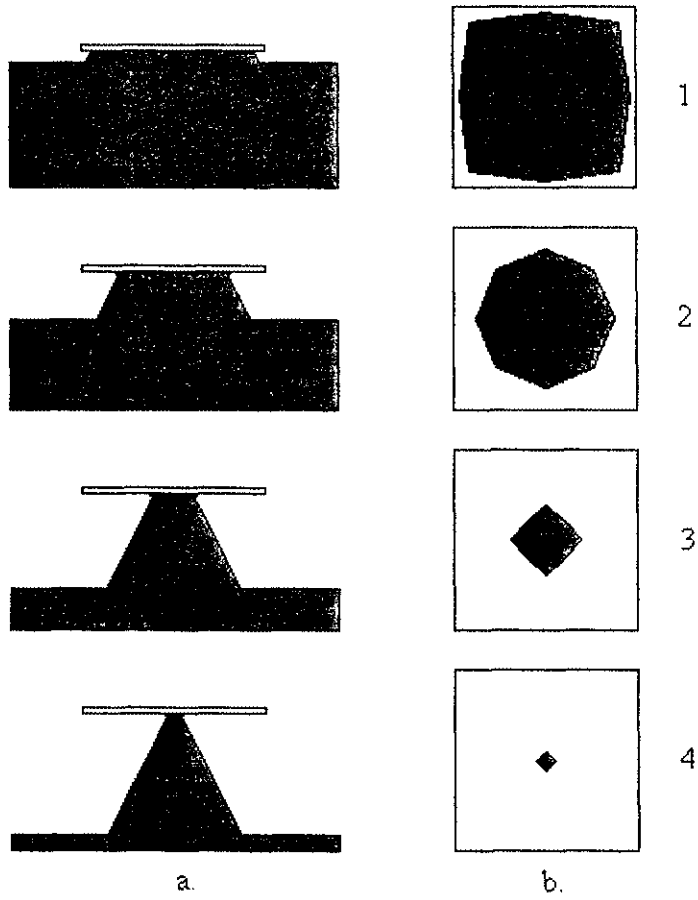


Figure 3.3: Schematic representation of the etch progress for a single pyramid tip. Column a. is a cross-section, and column b. is a top view of the tip as seen under an optical microscope. Row 1 represents the tip just after etching begins, and row 4 represents the final "oxide on" tip geometry.

3.1.2.3 Oxidation Sharpening

The outcome of this process step is an array of cusp shaped silicon nano-tips. The process step begins by cleaning the "oxide on" tip array in hot sulfuric acid followed by a rinse in deionized water. Extreme care must be taken so that the oxide squares are not broken off the tips. Next, the sample is oxidized using wet thermal oxidation at 1050°C for five hours. The goal of the oxidation is to convert the thin silicon neck connecting the

tip to oxide square to silicon dioxide. The oxide is then chemically removed using BHF to form the final nano-tip structure. This is shown schematically in figure 3.4.

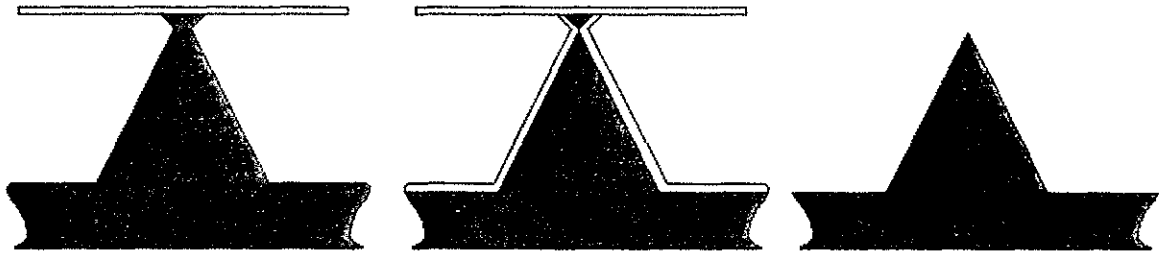


Figure 3.4: Schematic of the oxidation sharpening step for the new field emitter array fabrication process. a. An "oxide on" nano-tip. b. The oxidized "oxide on" tip. Note that the silicon neck is completely converted to silicon dioxide. c. The nano-tip after all silicon dioxide is removed.

3.2 Field emitter Uniformity Measurement

In order to determine if the new fabrication process produces more uniform field emitter arrays than the standard process in terms of nano-tip height variation, the following experiment was performed. Five field emitter arrays (400 tips per array) were fabricated according to the standard process and five according to the new process. For each field emitter array fabricated, the heights of 20 nano-tips were measured using scanning electron microscopy (SEM). To ensure that the sample set of tips chosen for measurement would represent the entire 20x20 array of nano-tips, nano-tips chosen for measurement were in a pattern similar to the pattern depicted in figure 3.5. To ensure that precise measurements were made on each sample, SEM parameters such as magnification, stage tilt, and sample orientation were the same for all measurements. The collected data was used to calculate the height standard deviation for each of the ten field emitter arrays. The results are used to compare the uniformity of the field emitter arrays

produced by each process. The set of arrays with the lowest tip height standard deviation is considered the most uniform set.

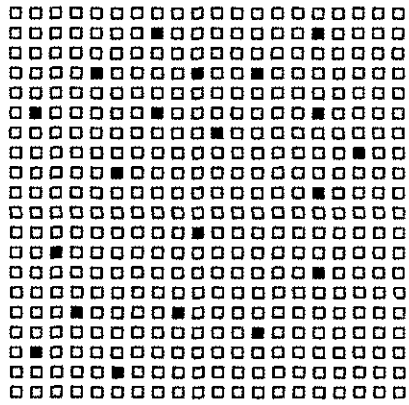


Figure 3.5: Example of a sample set of nano-tips chosen for height measurement from a 20x20 field emitter array. Each square represents the location of a tip, and the black squares represent a measured tip.

3.3 Field Emission Measurements

The goal of these measurements was to determine the field emission performance and consistency of field emitter arrays produced by the standard and new fabrication processes. The procedure for accomplishing this was to measure the I-V relation of 6 field emitter arrays produced by each process. The I-V relations were analyzed to determine the turn-on voltage, field enhancement factor, and emission area for each of the 12 field emitter arrays tested. This analysis is given in chapter 4. The resulting quantities will be used to decide if the new fabrication process has better field emission performance and consistency than the standard fabrication process.

3.3.1 I-V Test Set-up

The test set-up for obtaining the I-V relations consists of four main sections. The first section is the cathode-anode structure. The cathode is the field emitter array, and the anode is a flat piece of silicon. Electrical insulation between cathode and anode was created using mica. Mica was chosen for its excellent insulating properties and its ability to be cleaved into very thin layers. A 32-micron thick mica layer was used. The small spacing was used so that field emission could be achieved at voltages of less than 2kV. A schematic of the cathode-anode structure is given in figure 3.6.

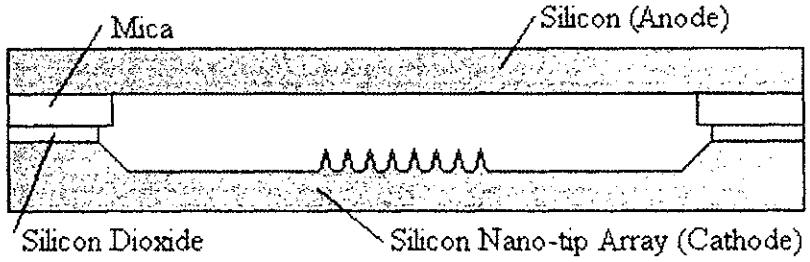


Figure 3.6: Cross-section of the cathode-anode structure used for I-V testing.

The second section is the field emitter array sample holder. The purpose of the sample holder was to provide a means to position and hold the field emitter array (cathode) directly in line with the anode and to provide a means of electrical connection to the cathode-anode structure. The sample holder is made of Teflon, an insulator. A schematic of the sample holder cross-section with cathode and anode in position is given in figure 3.7. The field emitter array and anode are positioned in the holder, and the clamping screws are tightened to pin and hold the sample in place. Electrical connection is made with the cathode by resting it on a silicon base plate mounted on the sample

holder. Electrical connection is made with the anode and silicon base plate by attaching a wire to the backside of each using conductive silver epoxy.

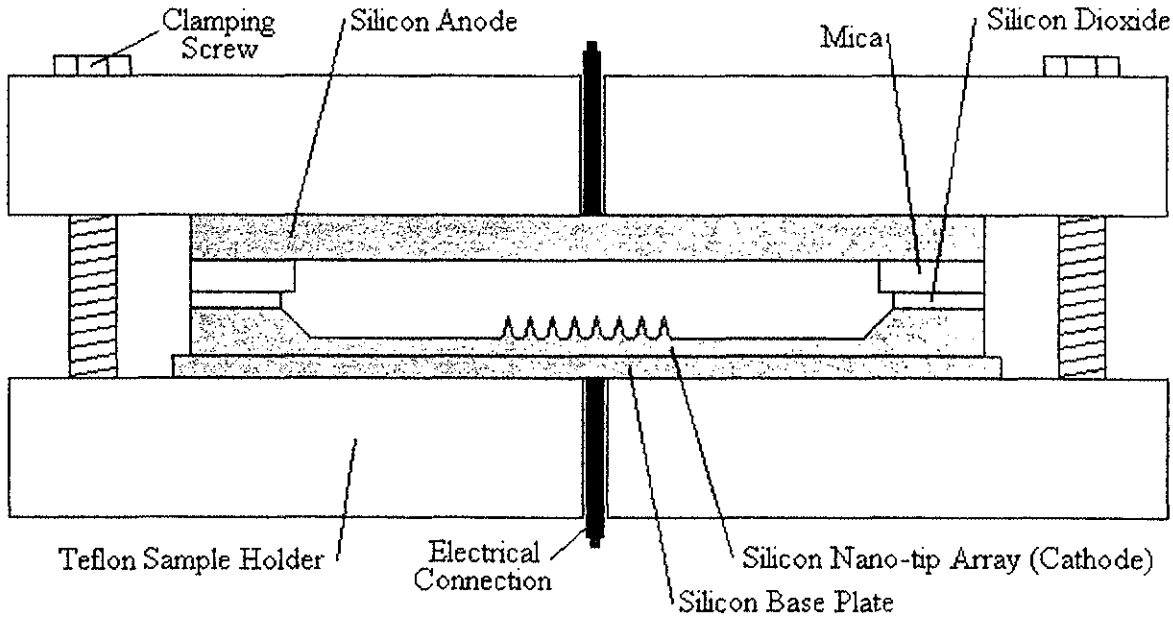


Figure 3.7: A cross-section of the sample holder used for I-V testing.

The third section of the I-V test set-up is the high vacuum system in which the I-V tests were performed. High vacuum is required so that the electron mean-free-path is made longer than the distance the electron must travel from cathode to anode. In addition high vacuum minimizes the chance of ionizing collisions between emitted electrons and air molecules. The resulting ions would be accelerated into the field emitters, creating damage and hence a permanent change in field emitter geometry. The vacuum system used is turbo-pumped backed by an oil-less scroll pump. The base pressure is approximately $1x10^{-8}$ Torr.

The final section of the I-V test set-up is the measurement equipment. The equipment consists of a high voltage source and an ammeter. A Keithley 247 high voltage source is used, which is capable of supplying up to 3kV. The ammeter used is a Keithley 2400, which is able to measure currents in the pico-amp range.

3.3.2 I-V Test Procedure

The I-V test procedure begins by dipping the field emitter array in dilute (2.5%) BHF for 5 seconds to remove any native silicon dioxide from the surface. Then the field emitter array and the anode are mounted in the sample holder as described above and placed in vacuum. A vacuum of $5x10^{-7}$ Torr or less is used. The high voltage source, the ammeter, and the cathode-anode structure are connected in series with a 10kΩ current limiting resistor as shown in figure 3.8.

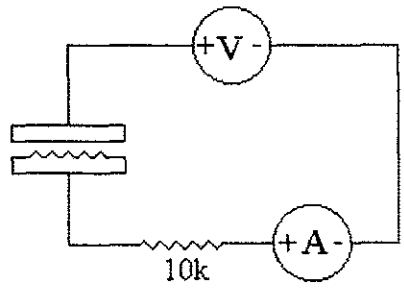


Figure 3.8: Circuit diagram of the I-V test set-up.

Before the I-V data was collected, the field emitter arrays were conditioned. A new field emitter array will have a thin layer of silicon dioxide or other contaminant on the surface, which can prevent emission. Conditioning is a process designed to overcome the emission blocking surface contaminants, and as a result it creates emission sites on the field emitter array. Without the conditioning process, the observed emission current

will be low up to some voltage, and then suddenly increase creating a discontinuity in the I-V data. Performing the conditioning process before I-V data is collected ensures that this jump in current will not be encountered. The conditioning process involved increasing the applied voltage from 500 volts up to 1500 volts in 100-volt increments. The voltage was held at each increment for 10 seconds.

After the conditioning process was complete, the I-V data was collected for each of the 12 samples as follows. The applied voltage was increased from 850 volts to 1800 volts in 50-volt increments. The voltage at each increment was held for 5 seconds, and then a current reading was taken. The voltage was increased from 850 to 1800 volts a total of three times for each sample. The average of the three current readings at each voltage was calculated and taken to be a point in the final I-V data for that sample.

CHAPTER IV

RESULTS AND DISCUSSION

Experiments designed to compare two nano-tip array fabrication processes were described in chapter 3. The experiments involved fabricating arrays and measuring the tip heights of a sample set of the nano-tips produced by each process. The tip height measurements were used to determine if the new fabrication process produced more uniform arrays than the standard fabrication process. Then, arrays fabricated by each process were used in field emission tests to determine any differences in field emission performance. In this chapter the results of these experiments are presented. A detailed analysis and discussion of the results is also given. The results of the standard and new fabrication processes along with the tip height measurements will be given. Using the tip height data, a statistical analysis will be performed to compare the tip height uniformity of each fabrication process. Finally, the results of the field emission testing will be given. From these results, it will be determined if the new fabrication process produces nano-tips arrays with better emission performance and consistency than the arrays produced by the standard process.

4.1 Standard Fabrication Process Results

Five nano-tip arrays, each containing 400 tips, were fabricated according to the standard fabrication process described in chapter 3. The shape of the as-etched nano-tips is pyramidal as given in figure 4.1, and the final geometry after oxidation sharpening is a cusp-shape as shown in figure 4.2.

For each nano-tip array, the heights of 20 nano-tips were measured using scanning electron microscopy. This data is presented in table 4.1. From this data, the average height of the nano-tips fabricated according to the standard process was calculated to be 1.78um with a height standard deviation of 0.1324um. The height average was calculated by taking the average height of the 20 measured nano-tips for each sample, and then averaging the five averages. The height standard deviation was calculated by taking the height standard deviation of the 20 measured nano-tips for each sample, and then averaging the standard deviations. The average of the height standard deviations is a measure of the tip-height height variation from sample to sample.

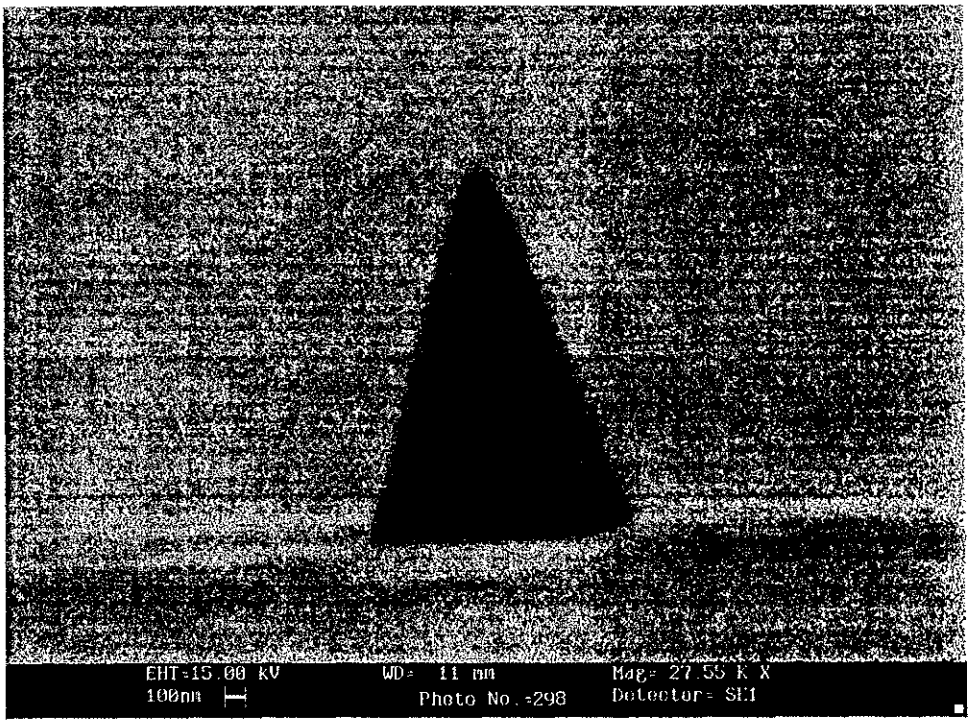


Figure 4.1: Scanning electron micrograph showing the pyramidal shape of the as-etched nano-tip fabricated according to the standard process.

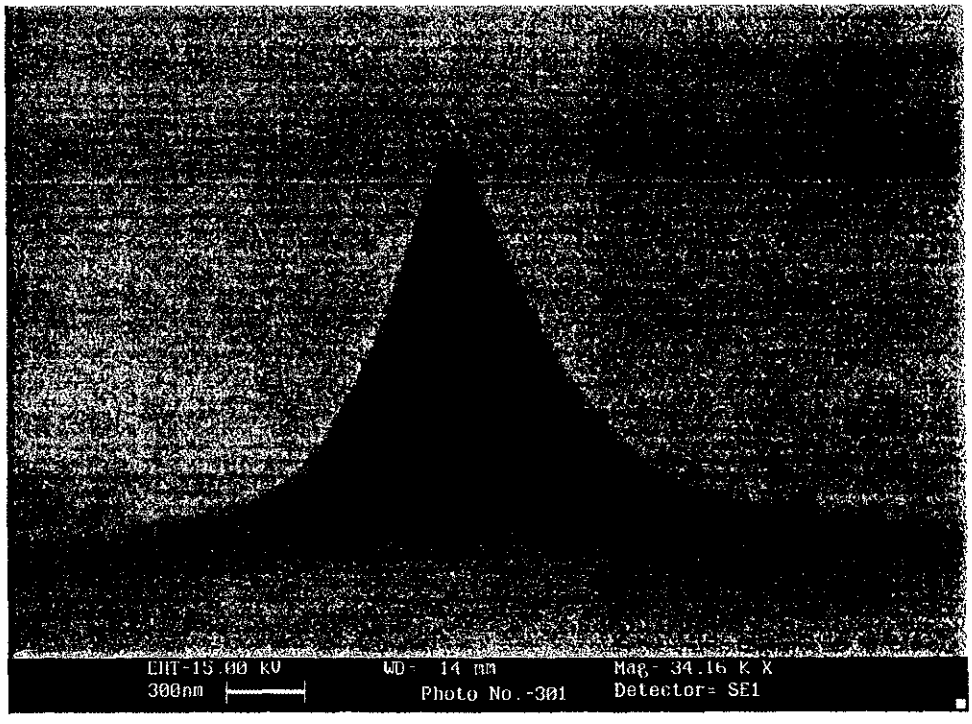


Figure 4.2: Scanning electron micrograph showing cusp-shape of a nano-tip fabricated according to the standard process.

Table 4.1: Raw tip height data in microns of 20 tips per array for five field emitter arrays fabricated according to the standard process.

Tip	A1 Height	A2 Height	A3 Height	A4 Height	A5 Height
1	1.84	1.62	2.13	1.72	1.75
2	1.79	1.82	2.08	1.81	1.67
3	1.51	1.91	2.14	1.8	1.78
4	1.77	1.7	2.04	1.44	1.86
5	1.66	1.63	2.05	1.6	1.77
6	1.64	1.79	1.66	1.65	1.97
7	1.5	1.77	1.82	1.8	1.96
8	1.86	1.94	1.87	1.86	1.78
9	1.53	1.81	1.72	1.49	1.72
10	1.87	1.94	1.7	1.77	1.88
11	1.57	1.95	1.65	1.71	1.84
12	1.85	1.84	1.72	1.55	1.75
13	1.86	1.92	1.75	1.82	1.72
14	1.73	1.78	1.56	1.71	1.86
15	1.79	1.97	1.89	1.69	1.76
16	1.68	1.91	1.45	1.71	1.73
17	1.72	1.81	1.75	1.44	1.66
18	1.66	1.89	1.94	1.77	1.75
19	1.78	1.83	1.8	1.79	1.68
20	1.82	1.94	1.65	1.86	1.49

4.2 New Fabrication Process Results

Five nano-tip arrays, each containing 400 tips, were fabricated according to the new fabrication process described in chapter 3. Figure 4.3 is a scanning electron micrograph of an "oxide on" nano-tip. The micrograph shows the hourglass shape of the thin silicon "neck" that connects the nano-tip to the oxide square. The pyramidal shape of the lower portion of the tip was expected and can be readily explained using orientation-dependent etching theory. The hourglass shape of the upper portion of the tip was unexpected, and is difficult to explain. It is speculated that the hourglass shape is caused by a reduction in the silicon etch rate at the silicon-silicon dioxide interface.

Figure 4.4 is a scanning electron micrograph of the nano-tip after the five-hour oxidation-sharpening step. Note the nano-tip is cusp-shaped, which is similar to the nano-tip produced by the standard fabrication process.

For each nano-tip array, the heights of 20 nano-tips were measured using scanning electron microscopy. This data is presented in table 4.2. From this data, the average height of the nano-tips fabricated according to the new process was calculated to be 1.47um with a height standard deviation of 0.0856um. The average height and standard deviation for the new process was calculated identically to the average height and standard deviation for the standard process as described above.

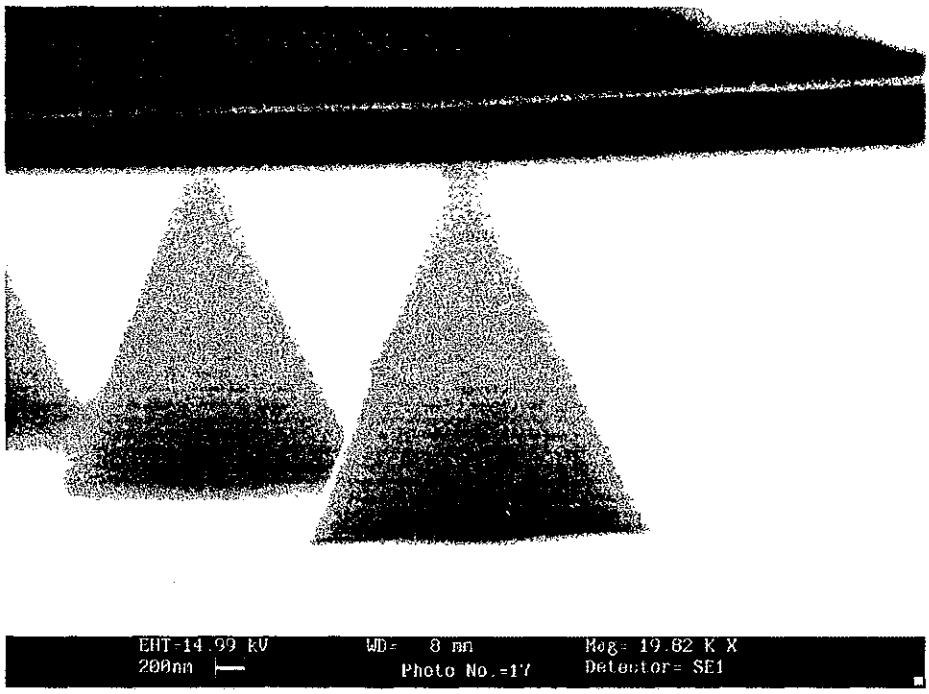


Figure 4.3: Scanning electron micrograph of an "oxide-on" nano-tip showing the hour-glass shaped thin silicon "neck" that connects nano-tip to the oxide square.

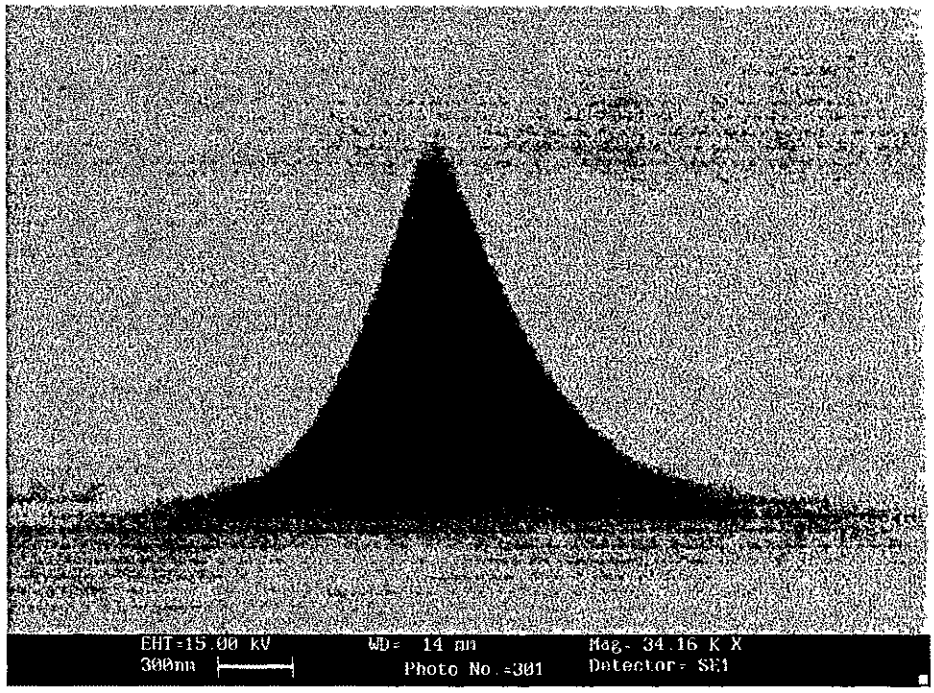


Figure 4.4: Scanning electron micrograph of nano-tip after the four-hour oxidation sharpening step. Note the tip's cusp-shape is the same tip shape produced by the standard fabrication process.

Table 4.2: Raw tip height data in microns of 20 tips per array for five nano-tip arrays fabricated according to the new process.

Tip	B1 Height	B2 Height	B3 Height	B4 Height	B5 Height
1	1.34	1.54	1.14	1.19	1.47
2	1.51	1.43	1.46	1.47	1.54
3	1.53	1.54	1.35	1.55	1.59
4	1.46	1.48	1.24	1.56	1.61
5	1.49	1.52	1.29	1.5	1.64
6	1.55	1.47	1.42	1.56	1.54
7	1.53	1.24	1.42	1.5	1.5
8	1.48	1.61	1.34	1.41	1.54
9	1.5	1.53	1.33	1.56	1.48
10	1.53	1.42	1.35	1.6	1.41
11	1.53	1.33	1.46	1.5	1.58
12	1.53	1.39	1.43	1.52	1.57
13	1.41	1.31	1.25	1.49	1.42
14	1.47	1.43	1.57	1.5	1.45
15	1.5	1.55	1.32	1.43	1.54
16	1.54	1.51	1.4	1.42	1.58
17	1.45	1.42	1.32	1.41	1.63
18	1.52	1.63	1.56	1.51	1.63
19	1.52	1.42	1.25	1.55	1.44
20	1.44	1.5	1.34	1.29	1.61

The result of the nano-tip height measurements show that the average height of nano-tips produced by the new process is 1.47um, which is 0.31um shorter than the average height nano-tips produced by the standard process. This height difference is accounted for in the following way.

First, consider nano-tips fabricated according to the standard process. The average height of the as-etched nano-tips measured using scanning electron microscopy is 1.9um. After the oxidation sharpening step the average nano-tip height is reduced to 1.78um. For the standard process, one hour of oxidation sharpening was used (one hour of oxidation produced a 0.4um layer of oxide), which corresponds to a 0.176um layer of silicon consumed. Subtracting the amount of silicon consumed from the as-etched tip

height (1.9um) results in a nano-tip height of 1.72um. This value is close (within 3.5%) to the average nano-tip height (1.78um) measured using the electron microscope.

Next, consider nano-tips fabricated according to the new process. The average dimensions of the "oxide on" nano-tips are as follows (refer to figure 4.5): h = 1.9um, w = 1.2um, n = 0.5um, and T = 1um where h is the 'oxide on' nano-tip height before oxidation, w is the width at the nano-tip's base before oxidation, n is the silicon neck width before oxidation, and T is the thickness of oxide grown during oxidation sharpening. The amount of tip height reduction due to oxidation sharpening is termed *r*. The equation for *r* derived from a geometric analysis of the 'oxide on' tip is

$$r = \left(\frac{0.44T}{\sin\left[\arctan\left\{2h/(w-n)\right\}\right]} - \frac{n}{2} \right)\left(\frac{2h}{w} \right).$$

Substituting the above values into the equation for *r* yields a tip height reduction due to oxidation sharpening of *r* = 0.63um. Subtracting the amount of height reduction from the original "oxide on" nano-tip height yields a final tip height of 1.27um. This value agrees reasonably well (to within 15%) with the average tip height of 1.47um measured using the electron microscope.

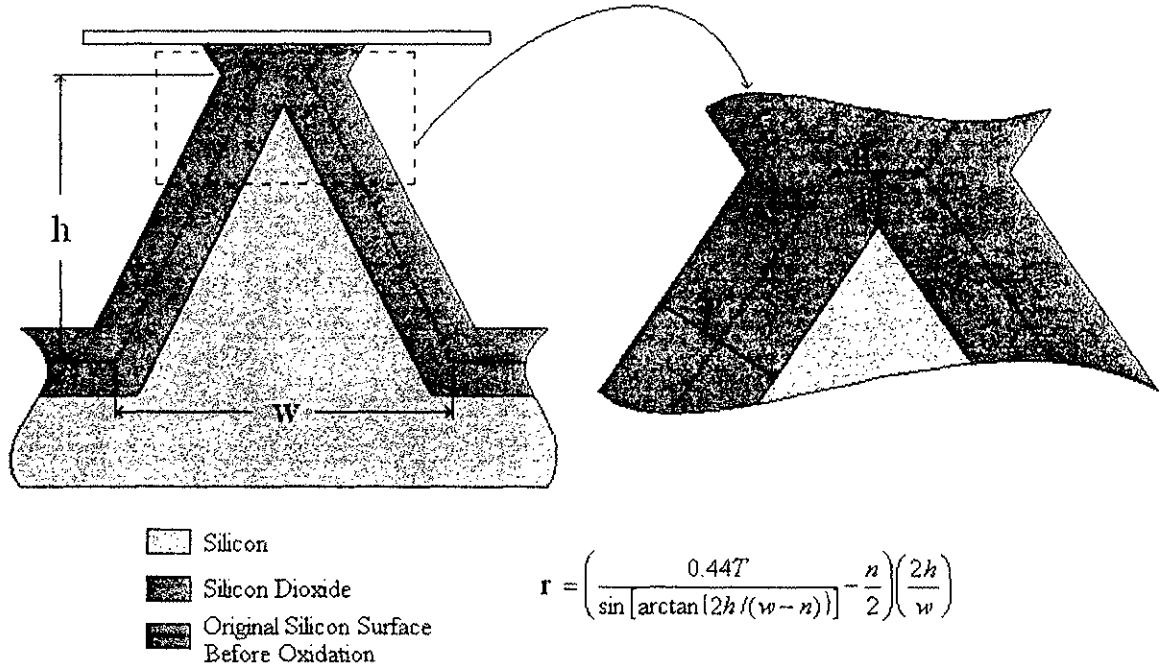


Figure 4.5: Schematic representation of "oxide on" nano-tip used to calculate the amount of tip height reduction r due to oxidation sharpening.

4.3 Analysis of Nano-tip Array Uniformity

As given above, the nano-tip height standard deviations were 0.1324um and 0.0856um for arrays produced by the standard and new processes respectively. From these results, at a first glance, it would be concluded that the new process produces more uniform arrays than the standard process. However, this conclusion was obtained from a sample population of nano-tips (not the entire population) and cannot be considered representative of the entire population without further statistical analysis of the nano-tip height measurements. Hence, the goal of this section is to validate the result using a statistical analysis of the nano-tip height data to convincingly show that the new fabrication process produces more uniform nano-tip arrays than the standard process.

The statistical analysis performed involves the computation of the 95% confidence interval for the true nano-tip height standard deviation for each fabrication process. This requires that the sampled values be from a normally distributed population [19]. In order to show this is the case for the population of nano-tip heights, the distribution of sample height values for each process were plotted against a normal probability distribution function (PDF). The normal PDFs used have as their average and standard deviation, the average and standard deviation calculated from the sampled values for each process. The averages and standard deviations were calculated by treating all 100 nano-tip height measurements for each process as the sample population. For the standard process the average and standard deviation is 1.77um and 0.144um respectively. For the new process the values are 1.47um and 0.104um respectively. The plots for the standard and new fabrication process are given in figures 4.6 and 4.7 respectively. As can be seen from the plots, the sampled tip height values from each fabrication process do indeed follow a normal distribution. From this, it is concluded that entire population of nano-tip heights is also normally distributed.

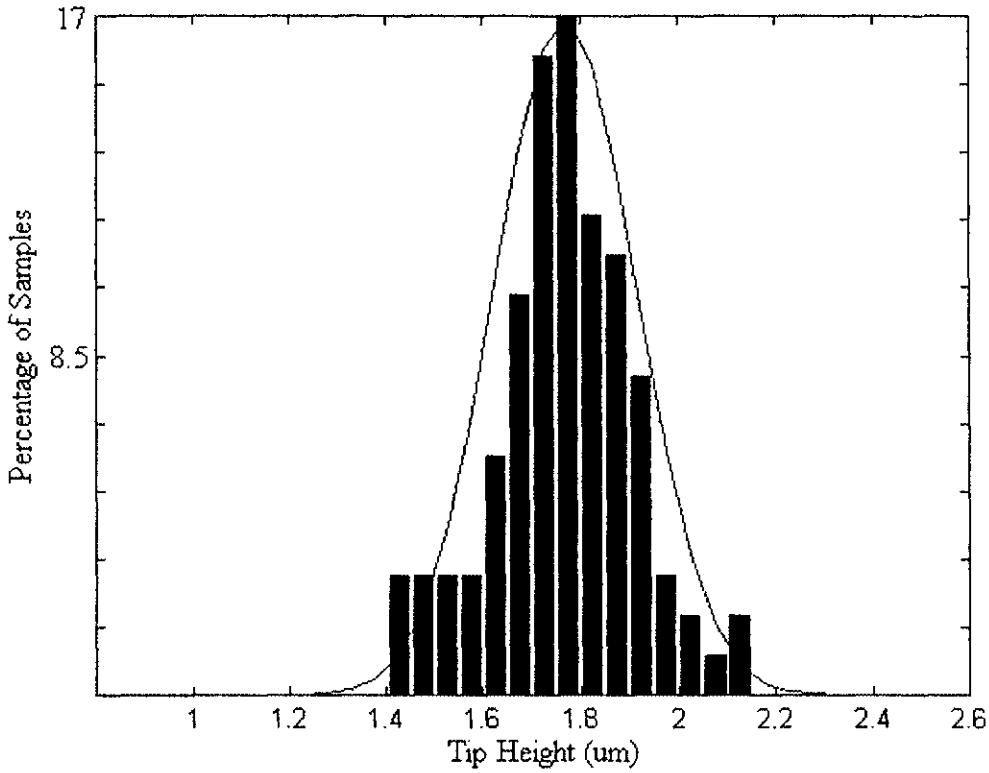


Figure 4.6: Nano-tip height sample distribution for arrays produces by the standard process plotted against a normal probability distribution function.

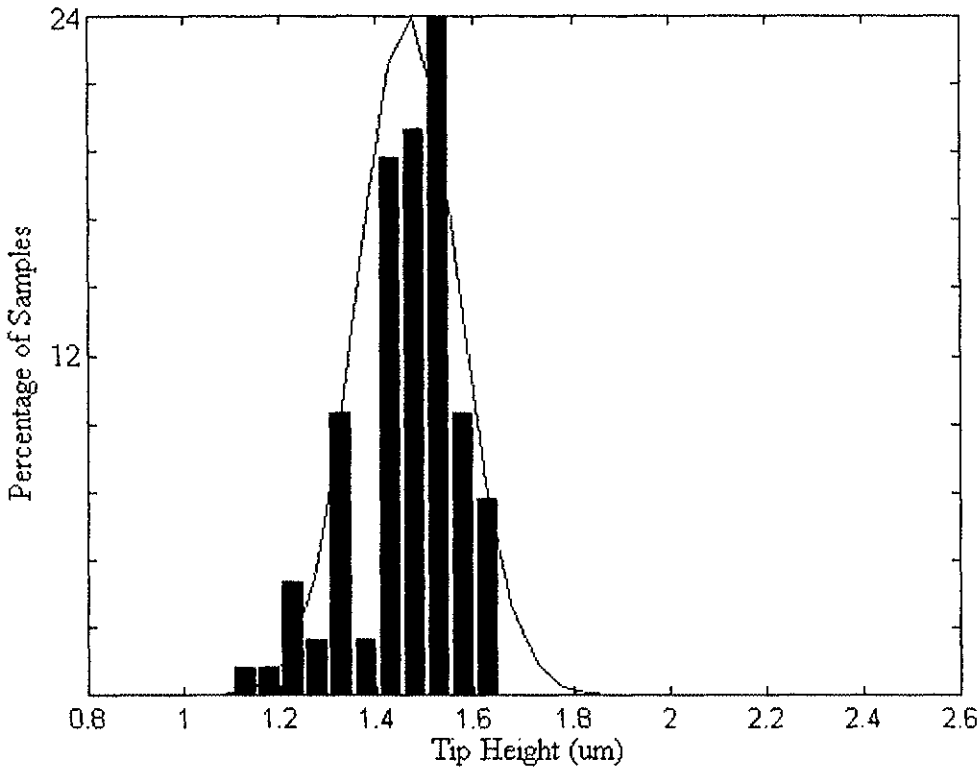


Figure 4.7: Nano-tip height sample distribution for arrays produced by the new process plotted against a normal probability distribution function.

Since the sample standard deviation ($\hat{\sigma}$) is being used as an estimate of the true standard deviation (σ), it is important to calculate the confidence interval for σ based on $\hat{\sigma}$. The confidence interval serves to fix an upper and lower limit on σ. If the 95% confidence interval is calculated for several sample populations, it will include σ 95% of the time and fail to include it 5% of the time.

The theory on which the confidence interval is based requires that the population sampled have roughly the shape of a normal distribution, which has already been shown to be true. The standard deviations of random samples from a normal population are not distributed normally or even symmetrically. It is true, however, that (N-1) $\hat{\sigma}^2/\sigma^2$

follows the chi-square (χ^2) distribution for N-1 degrees of freedom where N is the number of sample values [20]. From this it can be written,

$$\chi^2 = \frac{(N-1)\hat{\sigma}^2}{\sigma^2}.$$

To set up a confidence interval for σ based on this statistic, a few definitions must be given. First, α is defined in the following way. For a 0.95 (95%) confidence interval α = 1 - 0.95 = 0.05. Next, as shown in figure 4.6, $\chi^2_{\alpha/2}$ is defined as the value for which the area to the right under the chi-square distribution is equal to α/2. Likewise, $\chi^2_{1-\alpha/2}$ is the value for which the area to the left under the chi-square distribution is equal to α/2. Both values will depend on the number of degrees of freedom.

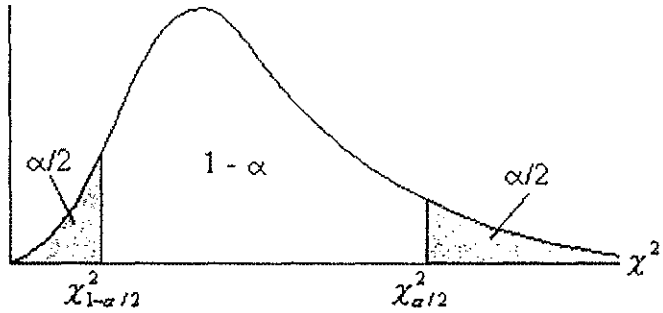


Figure 4.8: Chi-square distribution.

Referring to figure 4.8, it can be concluded with probability 1-α that a random variable having the chi-square distribution (in this case the nano-tip height standard deviation) will take on a value between $\chi^2_{1-\alpha/2}$ and $\chi^2_{\alpha/2}$. Using this result and the chi-square statistic for standard deviations given above, the following inequality can be written [19]:

$$\chi^2_{1-\alpha/2} < \frac{(N-1)\hat{\sigma}^2}{\sigma^2} < \chi^2_{\alpha/2}.$$

Rearranging this inequality yields the confidence interval for σ^2 which is:

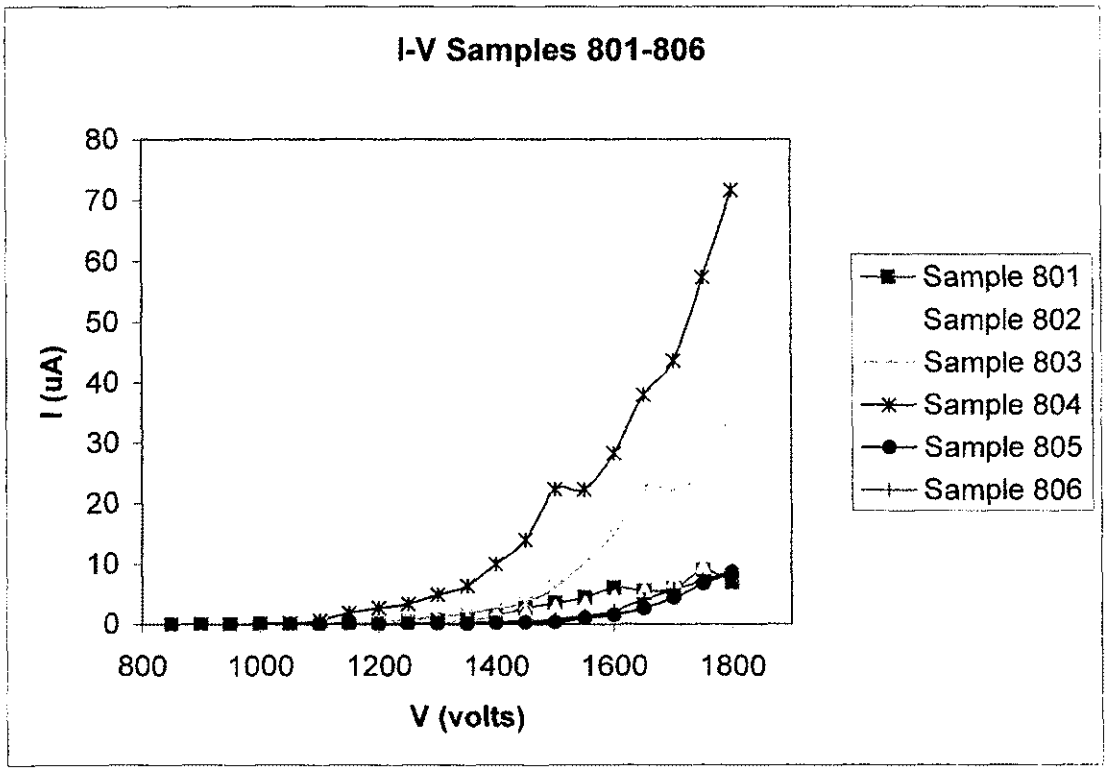
$$\frac{(N-1)\hat{\sigma}^2}{\chi^2_{\alpha/2}} < \sigma^2 < \frac{(N-1)\hat{\sigma}^2}{\chi^2_{1-\alpha/2}}.$$

Calculating the 95% confidence interval for the nano-tip height standard deviation for each process yields 0.1263um < σ < 0.1671um for the standard process and 0.09124um < σ < 0.1207um for the new process. Values used in the calculations are N = 100, α = 0.05, $\hat{\sigma}^2$ (as given above), and $\chi^2_{1-\alpha/2}$, $\chi^2_{\alpha/2}$ were taken from a table [20].

The results of the 95% confidence intervals for the nano-tip height standard deviations do indeed support the claim that the new process produces a more uniform nano-tip array than the standard process. This conclusion is made since the entire 95% confidence interval for the new process is less than the lowest value in the 95% confidence interval for the standard process.

4.4 Field Emission Test Results

The results of the field emission tests as described in chapter 3 section 4 will be given here. The test involved obtaining the I-V curves for six samples fabricated by the standard process and six by the new process. The I-V curves were then used to create Fowler-Nordheim (F-N) plots for each sample. The I-V and F-N data is given graphically in figure 4.9 and figure 4.10. Note that samples 701-706 were fabricated according to the new process, and samples 801-806 were fabricated according to the standard process.



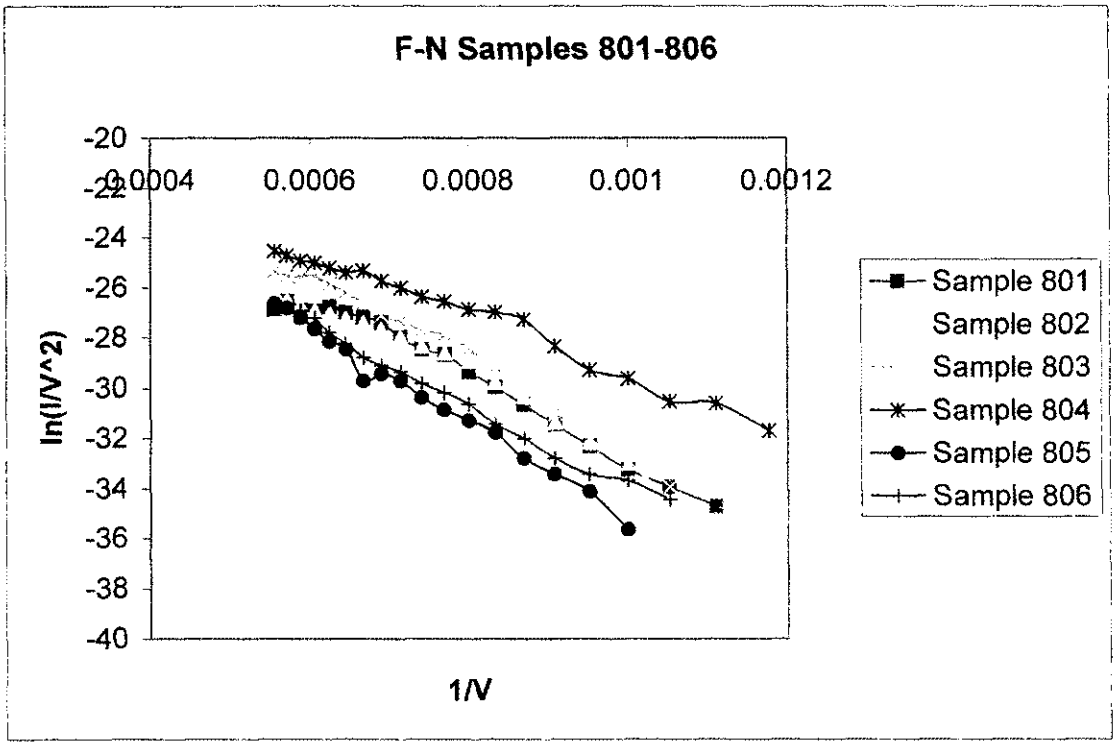
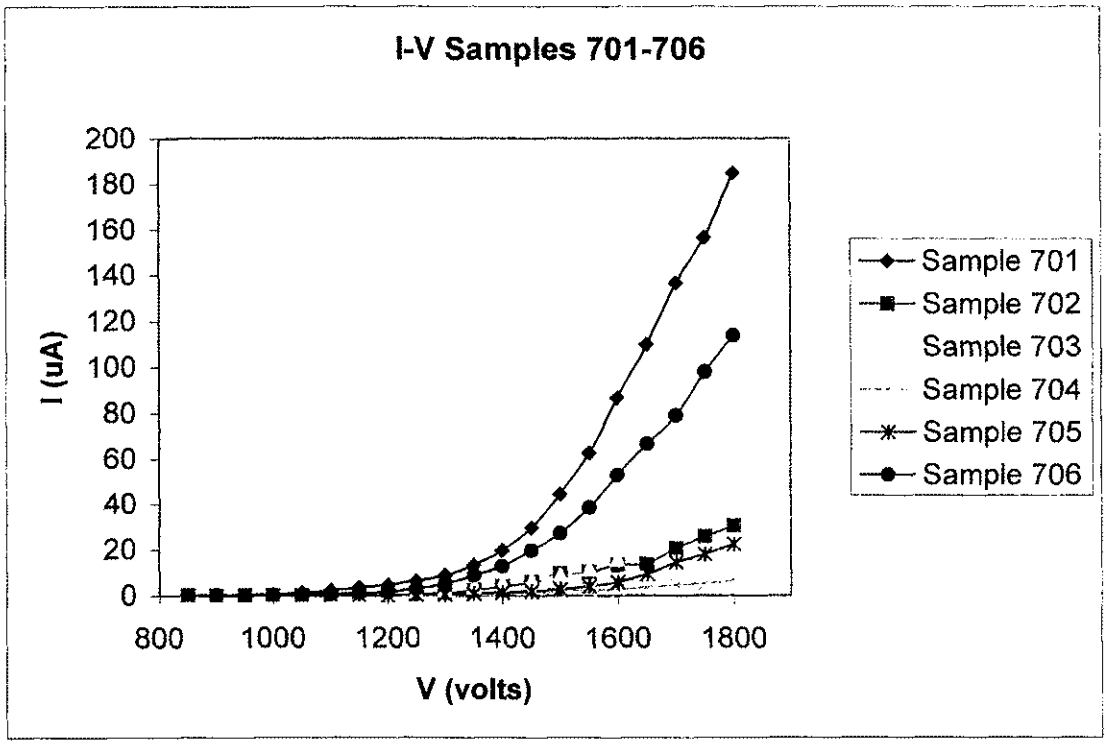


Figure 4.9: I-V and F-N plots for samples 801-806 (standard process samples).



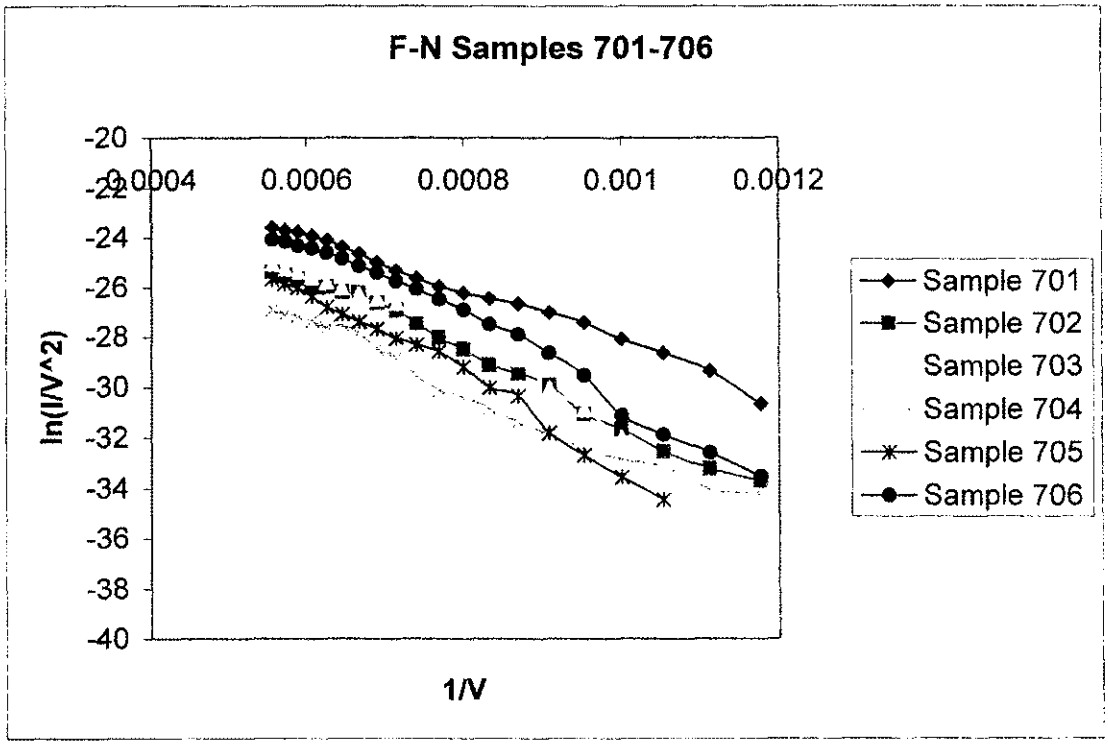


Figure 4.10: I-V and F-N plots for samples 701-706 (new process samples).

4.4.1 Turn-On Voltages

The turn-on voltage is defined as the voltage required to produce 5nA of field emission current. The turn-on voltage for each of the twelve samples is summarized in table 4.3. The average turn-on voltage for the new samples is 950 volts with a standard deviation of 114 volts. The average turn-on voltage for the standard samples is 1025 volts with a standard deviation of 121.45 volts.

These turn-on voltage values indicate that the new process produces better nano-tip arrays than the standard process. The lower average turn-on voltage for the nano-tip arrays produced by the new fabrication process is an indication that these nano-tips are sharper and therefore have a higher field enhancement factor. Also, smaller turn-on voltage standard deviation of the arrays produced by the new process is evidence that arrays produced by this process have better reproducibility than arrays made according to the standard process.

4.4.2 Fowler-Nordheim Plots

Plotting 1/V vs. $\ln(I/V^2)$ has yielded a relatively straight lines with negative slope for all samples. This is an indication that the observed current was a result of field emission. To extract the field enhancement factor and the emitting area from the plots, the straight-line equation of the F-N plot is required. Since the resulting F-N plots were not perfect lines, the method of least squares regression was used to calculate a trend-line that best fit the F-N data. The equation of the trend-line was then used to obtain the F-N slope (b) and y-intercept (ln a) for each sample.

Using the F-N slope and y-intercept for each sample, the field enhancement factor and the emitting area was calculated for each sample. As given in chapter 2, the field enhancement factor (β) was calculated using the equation

$$\beta = \frac{0.95B\phi^{3/2}}{b}$$

where B = $6.87x10^7$ and ϕ is the work function of silicon. The work function for n-type silicon of 0.005-0.020 Ω-cm resistivity was taken to be 4.27eV. This value was calculated using the work function difference (-0.17ev) between aluminum and 0.005-0.020 Ω-cm resistivity n-type silicon [18]. The work function difference was then subtracted from the work function for aluminum (4.1eV) to arrive at the work function for 0.005-0.020 Ω-cm resistivity n-type silicon.

Also in chapter 2, the emitting area (α) was given as

$$\alpha = \frac{1.1a\phi}{A\beta^2}\exp\left(-\frac{B(1.44x10^{-7})}{\phi^{1/2}}\right)$$

where A = $1.54x10^{-6}$. The F-N equations, field enhancement factor, and emitting area are summarized in table 4.3. In addition, the average and standard deviation of the field enhancement factor and the emitting area are given for each process.

The average field enhancement factor for arrays produced by the new and standard processes is $4.01x10^4$ and $3.67x10^4$ respectively. The higher field enhancement factor of the arrays produced by the new process is an indication that this process produces sharper (smaller radius of curvature at the nano-tip apex) nano-tips than the standard process. As further evidence of this, the average emitting area for each process is considered. Since field emission of electrons occurs mainly at the nano-tip apex, the emitting area should be smaller for sharper nano-tips. The average emitting area as

calculated using the equation above is 2.51×10^{-12} m^2 for the new process, which is 11% smaller than the emitting area of 2.83×10^{-12} m^2 for the standard process. Hence, the claim that the new process produces sharper nano-tips than the standard process is valid.

As a simple check of the emitting area, the following calculation was performed: Assume an array of 400 nano-tips whose radius of curvature at the tip apex is 25nm. (This value is roughly what one would expect for nano-tips produced by either fabrication process.) The area of one nano-tip apex is given by $2\pi r^2$ where r is the nano-tip radius of curvature. This turns out to be 3.93×10^{-15} m^2. This value multiplied by 400 (the total number of nano-tips) is 1.57×10^{-12} m^2 and is considered the total emitting area of the nano-tip array calculated from a geometric approach. So, the emitting area calculated from the F-N data is in close agreement with the emitting area calculated from a geometric approach.

As a final comparison of the standard and new fabrication processes, the amount of variation in the field enhancement factor and the emitting area are considered. The field enhancement standard deviation is 7.86×10^3 and 6.91×10^3 for the new and standard processes respectively. The larger amount of field enhancement variation in the new samples is evidence that the emission consistency of these samples may in fact not be any better than the standard samples.

In contrast to the result of field enhancement standard deviation is the variation in emitting area. It is expected that the variation in emitting area will be lower for samples with better emission consistency. The emitting area standard deviations are 3.36×10^{-12} m^2 and 4.62×10^{-12} m^2 for the new and standard samples respectively. The variation in the emitting area is lower for the new samples than for the standard samples.

To summarize, the results of the nano-tip height measurements and field emission tests have been given for samples produced by the new and standard processes. The data has been analyzed to determine if new process is better than the standard process in terms of uniformity and field emission performance. The factors used to draw conclusions were nano-tip height measurements (which included average tip height and tip height variation) and field emission measurements (which included turn-on voltage, turn-on voltage variation, field enhancement factor, field enhancement factor variation, emitting area, and emitting area variation). The results of the nano-tip height measurements indicate that the new process does produce more uniform arrays than the standard process. It is difficult to arrive at the same conclusion when considering the field emission data. While the field emission data does show some improvement in the new process over the standard process, the improvement can be said to be only marginal at best.

Sample #	Turn-On V	F-N Eqn.	ln(a)	a	b	ß (1/m)	α (m²)
		y = -bx + ln(a)					
701	750	y = -10694x - 17.53	-17.53	2.43E-08	-10694	5.38E+04	2.13E-13
702	950	y = -14500x - 16.94	-16.94	4.38E-08	-14500	3.97E+04	7.06E-13
703	1000	y = -16733x - 15.065	-15.07	2.87E-07	-16733	3.44E+04	6.15E-12
704	1000	y = -13073x - 19.61	-19.61	3.06E-09	-13073	4.41E+04	4.00E-14
705	1050	y = -17610x - 15.59	-15.59	1.70E-07	-17610	3.27E+04	4.05E-12
706	900	y = -15902x - 14.62	-14.62	4.48E-07	-15902	3.62E+04	8.69E-12
Average	941.67				-14752	4.02E+04	3.31E-12
StdDev	106.85				2560	7.84E+03	3.59E-12
801	1050	y = -15604x - 17.21	-17.21	3.36E-08	-15604	3.69E+04	6.28E-13
802	1050	y = -15591x - 17.15	-17.15	3.56E-08	-15591	3.69E+04	6.64E-13
803	1000	y = -18170x - 14.56	-14.56	4.76E-07	-18170	3.17E+04	1.20E-11
804	800	y = -11618x - 17.82	-17.82	1.82E-08	-11618	4.96E+04	1.88E-13
805	1150	y = -19218x - 16.07	-16.07	1.05E-07	-19218	3.00E+04	2.98E-12
806	1100	y = -16464x - 17.53	-17.53	2.44E-08	-16464	3.50E+04	5.08E-13
Average	1025.00				-16111	3.67E+04	2.83E-12
StdDev	121.45				2636	6.91E+03	4.62E-12

Table 4.3: Summary of I-V and F-N data for samples 701-706 and 801-806 including turn-on voltages, field enhancement factor (β), and emitting area (α).

CHAPTER V

CONCLUSIONS

In this thesis the effect of geometric uniformity on the field emission performance of silicon field emitter arrays was investigated. This was achieved by fabricating arrays according to two separate processes termed the standard process and the new process. The new process was designed to produce more uniform arrays than the standard process. The uniformity of the arrays produced by each process was verified experimentally. To determine the effect of array uniformity on field emission performance, arrays produced by each fabrication process were used in field emission tests.

5.1 Array Fabrication

Both types of field emitter arrays were fabricated on n-type <100> silicon wafers using standard silicon processing techniques. The techniques included thermal silicon oxidation, photolithography, and wet anisotropic silicon etching. For each process an array of silicon dioxide squares was used as a masking layer during wet anisotropic silicon etching. Silicon etching created a silicon tip at the location of each silicon dioxide square.

The distinct difference between the standard process and the new process is in the silicon etch step. In the standard process, the silicon etch step continued until the oxide squares were removed from the tips. In the new process, silicon etching was stopped just

prior to removal of the oxide squares. This technique prevents any etching of the top of the tips, resulting in arrays with better tip height uniformity than arrays fabricated according to the standard process.

During testing of the array fabrication processes, examination of the as-etched tip with oxide mask attached revealed that the thin silicon region connecting the tip to the oxide square was hourglass shaped (see figure 4.3) rather than the expected pyramidal shape. Although there is no sure explanation for this geometry using the theory presented in chapter 2, it is speculated that it is due to a decreased silicon etch rate at the silicon-silicon dioxide interface.

For both processes, the array of as-etched tips were oxidation sharpened. In a previous study it was found for the standard process that one-hour of silicon oxidation optimized the oxidation sharpening step by minimizing tip height reduction while maximizing tip sharpness [16]. For the new process the oxidation sharpening time used was 5 hours for a silicon neck width of 0.5um.

5.2 Array Uniformity Measurements

To verify that the new process produced more uniform arrays than the standard process an experiment was performed. The experiment involved fabricating five arrays according to the standard process and five according to the new process. The heights of a sample population of tips were measured for each set of five arrays. A statistical analysis was performed on the tip height data to gauge the uniformity of the arrays produced by each process.

Analysis of the tip height data included calculating average tip height, tip height standard deviation, and the 95% confidence intervals for the height standard deviation. It was found that tips produced by the standard process were 0.31um taller than tips produced by the new process. The difference is due to a larger amount of tip height reduction produced by the new process's oxidation sharpening step. The tip height standard deviation confirmed that the new process produces more uniform arrays than the standard process. This conclusion is based on the fact that the sample height standard deviation for the new process was 27% less than the height standard deviation for the standard process. The 95% confidence intervals for the height standard deviation provide further evidence in support of the above conclusion. The maximum of the 95% confidence interval for tips produced by the new process is less than the minimum of the 95% confidence interval for tips produced by the standard process. This result states that 95% of the time the true height standard deviation of arrays produced by the new process will always be less than the true height standard deviation of arrays produced by the standard process.

5.3 Field Emission Measurements

Once it was determined that the new process produced arrays with better tip height uniformity than arrays produced by the standard process, a field emission experiment was performed to determine the effect of array uniformity on field emission performance. The experiment involved fabricating six arrays according to the standard process and six according to the new process. Next, the field emission current-voltage relationship was measured for each array using the procedure described in chapter 3. The

current-voltage relationship was then used to calculate the F-N relation for each array. Using the current-voltage and F-N data the turn-on voltage, emitting area, field enhancement factor, and the corresponding standard deviations of each quantity were determined for each of the 12 arrays. These quantities were used to analyze the field emission performance of the arrays produced by each process.

Analysis of the above quantities has revealed a marginal improvement in field emission performance of the new arrays over the standard arrays. Improvement was defined in terms lower turn-on voltages, higher field enhancement factors, and lower standard deviations in turn-on voltage, field enhancement factor, and emitting area. With the exception of field enhancement factor standard deviation, the new arrays displayed improvement over the standard arrays in all categories.

The average field enhancement factor for arrays fabricated according to the new and standard processes was 4.02×10^4 and 3.67×10^4 respectively. Recall the relation

$$\beta \propto \frac{2h/r}{\ln(4h/r) - 2}$$

presented in chapter 2 section 3.3.1 where h is the height of the emitter tip and r is the radius of curvature at the apex of the emitter tip. This relation states that the field enhancement factor should increase with tip height. However, it was determined that the new process, which produces shorter tips than the standard process, has the larger field enhancement factor. Therefore, it is concluded that tips produced by the new process are sharper than tips produced by the standard process (i.e. the new tips have a smaller radius of curvature at the apex).

Using the relation above, the ratio of the average field enhancement factor for the standard process (β_2) to the average field enhancement factor for the new process (β_1) is

$$\frac{\beta_1}{\beta_2} = \frac{h_1 r_2[\ln(4h_2/r_2)-2]}{h_{21} r_1[\ln(4h_1/r_1)-2]}.$$

Since h>>r, and the natural log terms vary slowly with changes in h and r, their ratio is approximated as unity. Therefore, the relation reduces to

$$\frac{\beta_1 h_2}{\beta_2 h_1} = \frac{r_2}{r_1}.$$

Making the substitutions for β_1, β_2, h_1=1.47um, and h_2=1.77um (where subscript 1 represents values for the new process and subscript 2 represents values for the standard process) it is determined that $r_2=1.32r_1$ which supports the conclusion that tips produced by the new process are sharper than tips produced by the standard process.

5.4 Future Work

Silicon is an ideal substrate material for other field emission materials due to its ability to be micromachined. An array of silicon tips can be coated with a suitable field emission material and due to the geometry, the silicon tips will provide a large field enhancement factor lowering the voltage required to for emission of electrons from the coating material. As shown in this thesis however, non-uniformities in the silicon substrate will degrade field emission performance and consistency from sample to sample. For this reason, methods to fabricate high uniformity silicon arrays need to be explored further.

The fabrication processes presented in this thesis used wet anisotropic etching to create the tips. Wet etching is a difficult process to control due to difficulty in detecting the endpoint and due to variations in etch rate date caused by etchant temperature and concentration fluctuations. For these reasons, replacing the wet etch step with a dry etch

process would be advantageous since dry etching allows a much higher degree of uniformity to be achieved.

Other future work includes investigation of the hourglass shaped structure produced at the silicon-silicon dioxide interface during wet anisotropic silicon etching. If further utilization of this phenomenon is to be realized, the conditions under which these phenomenon can be produced (i.e., etching parameters, silicon doping concentration, etch mask materials, etch mask shapes, etc.) and if the size of the hourglass is scalable or fixed need to be determined. Investigation of the hourglass phenomena may lead to previously unrealizable structures in silicon, leading to useful applications and new devices.

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