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Modeling Leakage Currents in Metal Insulator Metal Structures with High K Materials

Priyamvada Maleeswaran
Old Dominion University

MODELING LEAKAGE CURRENTS IN METAL INSULATOR METAL STRUCTURES WITH HIGH K MATERIALS

by

Priyamvada Maleeswaran
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Approved by:

Ravindra P. Joshi (Director)

Sylvain Marsillac (Member)

Gene Hou (Member)

ABSTRACT

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Priyamvada Maleeswaran
Old Dominion University, 2012
Director: Dr. Ravindra P. Joshi

Various products such as personal computers, cellular phones and mobile devices require high speed and low power consumption. Such improvements have been attained by minimizing physical dimensions of electronic devices, leading to high density integration of transistors and capacitors on integrated chips (ICs). However, as a consequence of down-scaling device dimensions, tunneling of electrons through thin gate oxides (SiO_2) increases, leading to increased static power leakage. This constitutes wastage in power, and for the case of memory applications necessitates faster refresh cycles. In order to overcome such issues, high-*k* materials (such as HfO_2 and ZrO_2) that allow physically thicker films and reduce leakage current while maintaining gate capacitance have been proposed. Unfortunately, high-*k* materials have high defect densities that give rise to trap levels within the semiconductor band gap and open pathways for leakage currents. Such leakage currents are detrimental in Metal-Insulator-Metal capacitors that are the next generation capacitors for Radio Frequency (RF), DRAM (Dynamic Random Access Memory), and analog/mixed signal ICs applications. Hence, a detailed understanding of transport process is required to predict the dominant leakage current mechanism in high- *k* materials. In this research, a complete transport picture is presented by accounting for electron flow through the high- *k* oxides including trap-assisted transport. Other conduction mechanisms such as direct tunneling, Fowler-Nordheim (FN) tunneling and elastic trap assisted tunneling have also been considered to provide a complete model that can determine the leakage current density as a function of applied voltage or electric fields. For completeness, analyses for the material

parameters (e.g., the optical permittivity) were carried out based on a commercial software package (CASTEP). This material analysis package uses density functional theory. The overall model has been validated with experimental data for $Cr/HfO_2/Cr$ and $TiN/ZrO_2/TiN$ structures. The leakage current densities in these materials agree well with the experimental data published.

I dedicate this thesis to my family, my thesis advisor, and God for all the love, blessings, support and strength.

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CHAPTER 1

INTRODUCTION

1.1 MOTIVATION

The usefulness of the Si/SiO_2 gate dielectric system was first demonstrated in 1957 in Silicon MOS transistors (ref). Since then, the fundamental device structure and materials have not changed although the sizes of the transistors have been reduced significantly. This aggressive scaling has led to increased transistor per integrated circuit which is best observed by Moore's Law. Moore's Law states that over the history of computing hardware, the number of transistors on an integrated chip doubles every two years. This trend is expected to continue until at least the year 2015 or 2020. According to the 2010 update of International Technology Roadmap for Semiconductors, the historical 2 year doubling trend is expected to have slower growth (transistor doubling about every 3 years) as shown in Fig. 1.

This slower growth rate in Moore's Law is due to the shrinking dimensions of transistors that require many difficult challenges to be overcome. In particular, the gate dielectric material SiO_2 will reach a fundamental scaling limit due to increasejkmjmnm n gate leakage current, thus presenting a challenge to continued scaling. For poly $Si/SiO_2/Si$ with a gate bias of 1 V, the leakage current increases from 10^{-6} A/cm^2 for a 3 nm SiO_2 layer to 10 A/cm^2 for a 1.5 nm SiO_2 layer [1]. The high gate leakage current alters device performance and increases standby power consumption. Therefore, reducing leakage current has played an important role and is critical in the search for alternatives to SiO_2 based gate dielectrics. In recent years, research efforts have been focused on developing alternative high-*k* materials to replace SiO_2. The challenge of replacing a material (SiO_2) that has proved advantageous over the past 40 years has led to the research and development of novel computational and processing approaches.

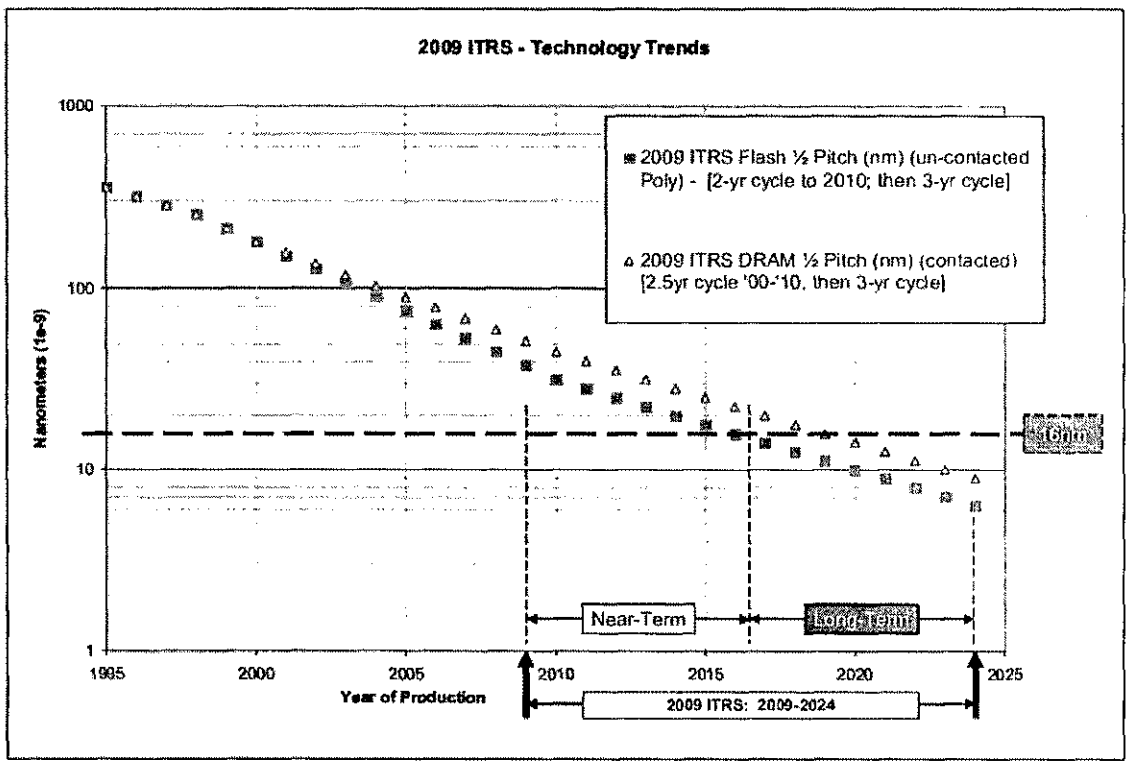


Figure 1: Technology trend following Moore's Law (ITRS) [2].

Simulations at the atomic scale can computationally predict properties of materials based on microscopic interactions between atoms and electrons in the system. Many different materials such as Al_2O_3, HfO_2, ZrO_2, TiO_2, and $SrTiO_3$ have been investigated to study their band structure, density of states, and material properties with the aim to reduce undesirable leakage currents [1]. Extensive research has been done on Metal-Insulator-Metal structures as such material systems can meet the need of next generation DRAM capacitors. Imec (Interuniversity Microelectronic Center) performs world-leading research in nanoelectronics and nanotechnology and has launched MIM capacitor for DRAM applications program to focus on optimization of dielectric systems.

Using the physical properties of high-*k* materials, a model for electronic transport to predict the magnitude of leakage current and its underlying process in MIM structures has been the focus of our research. Although many models such as Trap Assisted Tunneling, Poole Frenkel

emission, etc. have been proposed based on the material under consideration, existing models have failed to provide a complete picture of transport [3]. A model encompassing a complete current transport picture is necessary to predict and quantify the dominant leakage current mechanisms for different materials at different applied biases. Therefore, the aim of this research is to understand transport processes and incorporate the carrier transitions in and out of traps to provide a complete transport picture in Metal-Insulator-Metal structures for determining dominant current conduction mechanism and simulating leakage current density as a function of applied bias in high k materials.

1.2 SCOPE AND ORGANIZATION

In order to observe the complete transport picture in high dielectric materials, leakage current mechanisms in an MIM structure are studied. This research primarily focuses on HfO_2 as the oxide/insulator and Chromium as the metal electrode.

This thesis is organized as follows.

Chapter 2 reviews the history, operation and fabrication associated with MOSFET along with its use in integrated circuits. The effect of scaling and its associated limiting factors/challenges are also discussed with regard to semiconductor devices such as MOSFETs, heterostructures, and MIM capacitors. The current solution to overcome the challenges, i.e. to replace gate material with high-*k* materials to improve the performance in semiconductor devices, is presented. Lastly, this chapter includes the possible materials, advantages and challenges in high k technology leading to the motivation of this research.

Chapter 3 focuses on the methodology adopted to model the current transport mechanisms in high k materials. The derivation of materials' properties such as band gap, density of states, optical permittivity, etc. that are based on the electronic structure of high-k materials is also discussed.

Chapter 4 presents the results from our simulations using the models in chapter 3. The quantum mechanical models of current conduction mechanisms to predict the gate leakage

current density in hafnium oxide (HfO_2) are analyzed based on electric field, thickness of gate oxide, barrier height, trap levels, defect density, and other material parameters. The simulated leakage current density is validated with experimental data for hafnium oxide (Cr/HfO_2) and zirconium oxide ($TiN/ZrO_2/TiN$). The theoretical predictions are shown to be in good agreement with the data, thus enabling quantitative predictions of the relative strengths of the contributing mechanisms.

Chapter 5 encloses the summary of this research and discusses the scope for possible future work that could be undertaken for further analyses and research evaluation.

CHAPTER 2

BACKGROUND AND LITERATURE SURVEY

2.1 INTRODUCTION

This chapter briefly reviews the importance and challenges associated with gate oxide scaling to motivate the need for modeling high-k materials and their current transport mechanisms. Devices such as Metal Oxide Semiconductor Field Effect Transistors (MOSFETs), hetero structures, and Metal Insulator Metal (MIM) structures are reviewed to underscore the need and importance of using high-dielectric oxides. Advances that have taken place in a wide variety of applications that use high-k technology are also briefly reviewed in this chapter.

Section 2.1 begins with the history and applications of MOSFETs-- a major component in integrated chip fabrication. Followed by its operation, this section reviews the effect of scaling and the associated limiting factors. Next, a brief background of possible materials is given in Section 2.2. Section 2.3 then describes heterostructures and their applications. In this context, the phenomenon of current collapse is also reviewed to capture an important issue and in understanding the mechanism behind this observed phenomena. As will be discussed, traps are thought to contribute to this process. Section 2.4 describes MIM structures along with their applications and targets the dielectric constant as an important parameter that requires improvements. The fabrication method is also briefly discussed to show that this advancement will not be possible without reliable and high quality manufacturing processes. Furthermore, this section also reviews a few proposed high-k dielectric materials for nanocapacitor applications. The established relation of capacitance to dielectric constant for these materials is presented. Section 2.5 deals with high-k materials, their uses and challenges for the semiconductor industry with some relevant terms, and transport mechanisms. Further the motivation and purpose of the present research is also stated in this section.

2.1 MOSFETs

The Metal Oxide Semiconductor Field Effect Transistor (MOSFET) is a unipolar three terminal device that acts as a switch by either connecting or isolating the source (S) and drain (D) based on the applied voltage at the gate (G). The gate sits over an oxide layer, which traditionally has been SiO_2 for silicon based technology.

2.1.1 History and Applications

MOSFETs were first fabricated in 1960 by using thermal oxidation on a silicon substrate. They had a channel length of about 20 μm and gate oxide thickness of 100 nm [4]. Present day MOSFETs are scaled down considerably. Due to scalability, low power consumption and high yield of working devices, MOSFETs are the most important devices for advanced integrated circuits and semiconductor memories. Other applications of MOS diodes are storage capacitors and charge coupled devices (CCDs) whose principle involves charge storage & transfer actions controlled by gate electrodes. CCDs are used in image sensing and signal processing [4].

2.1.2 MOSFET Operation

MOSFET is composed of a Metal Oxide Semiconductor (MOS) diode (as shown in Fig.2) and has two p-n junctions placed immediately adjacent to the MOS diode.

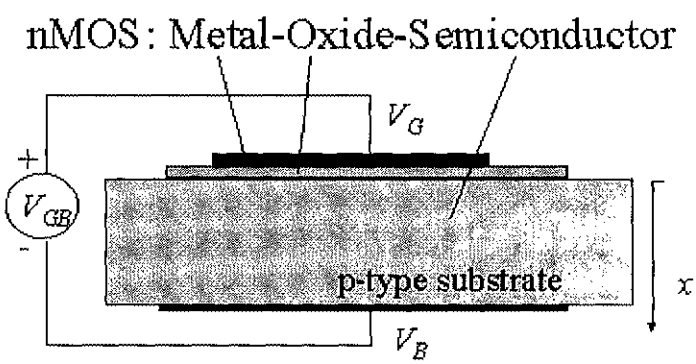


Figure 2: The MOS structure [5].

The switching action of MOSFET is achieved by a gate capacitor, and it depends on the polarity of the voltage applied. The gate voltage then induces (via a field effect) a positive or negative charge in the channel region along the bottom plate of the gate capacitor. It is the channel charge (comprised the majority carriers) that determines the connectivity of the source and drain. The type of channel charge depends on the type of MOSFET, which could either be a n-channel MOSFET or a p-channel MOSFET. An NMOS has a p-type semiconductor substrate in which two n+ regions, the source and drain, are formed. The gate oxide is usually SiO_2, and the metal plate on the oxide is called the gate. The majority carriers in the channel between source and drain in NMOS are electrons.

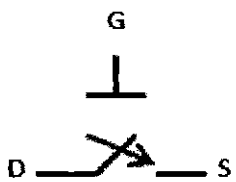


Figure 3: MOSFET as a switch.

The amount of charge (Q) induced in the channel region of a MOSFET is the product of gate oxide capacitance (C_{ox}) and the voltage drop across the gate capacitor (V).

$$Q = C_{ox} V \,, \tag{2.1}$$

C_{ox} can be modeled as the capacitance of a parallel plate capacitor and is given by:

$$C_{ox} = \frac{k_{ox}\varepsilon_0 A}{t_{ox}} \,, \tag{2.2}$$

where k_{ox} is the relative dielectric constant, ε_0 is the permittivity of free space, A is area of the capacitor/gate oxide, and t_{ox} is the physical thickness of dielectric material.

The drain-source current for long channel MOSFET operating in the saturation region is given by:

$$I_{DS} = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{gs} - V_t)^2 \,, \tag{2.3}$$

where μ is the channel mobility, W and L are the width and length of the channel region, respectively, V_{gs} is the gate-source potential, and V_t is the threshold voltage.

2.1.3 Gate Oxide Scaling Limits

Equations (2.2) and (2.3) reveal that reducing the lateral (L) and the thickness of the oxide (t_{ox}) in the device increases the current flow between the drain and source. This is because reducing t_{ox} increases C_{ox} and hence the amount of channel charges. Reducing L decreases the distance the channel charge must travel to conduct a current leading to faster switching time. This ability to continually shrink critical dimensions of the MOSFET to increase performance is referred to as scaling. Scaling transistors to small dimensions has played a major part in the success of CMOS technology in integrated circuits. Scaling has been a primary factor in decreasing transistor delay times by more than 30% per technology generation [7]. This has resulted in doubling of microprocessor performance every two years along with reduced power consumption. However, a roadblock was reported (as discussed next) that could limit the scaling of gate oxide thickness for improved device performance.

SiO_2 (or nitrided SiO_2) have been used as a gate dielectric for over 40 years in the semiconductor industry owing to its manufacturability and ability to deliver improved device performance by making it thinner. Besides, being a native oxide for silicon makes the device fabrication an easier process. Conventional scaling of critical dimensions in MOSFET have enabled gate size reduction from 10 μm in the 1970's to a size of 0.1 μm in the beginning of the 21st Century [7]. Over the last few decades, tremendous improvements in processing have produced high-quality SiO_2 layers with the required thickness and very few electronic defects in amorphous structure and forms an excellent interface with Si. However, the fundamental thickness limitation for SiO_2 gate oxide layers of ~1.2 nm was reached a number of years ago based on the tunneling currents. Other impediments to further downscaling include oxide leakage and breakdown and the requirement for control of the channel current by the gate. In the

following section, a brief overview of oxide leakage and breakdown is provided as these effects play a major role in determining the fundamental scaling limit of SiO_2.

2.1.4 Oxide Leakage Current Due to Tunneling

When a high electric field is applied to a p-n junction in the reverse direction, a valance electron can make a transition to the conduction band, by penetrating through the band gap. This effect is called tunneling (Fig. 4).

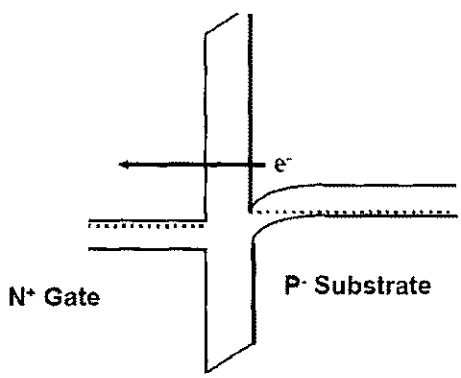


Figure 4: Direct tunneling leakage mechanism for thin SiO_2 [7].

As the thickness of gate material decreases due to increase in electric field (refer equation 2.4) direct tunneling of charges through potential barriers occurs at lower voltages. Due to difference in barrier height for electrons and holes, and higher tunneling probability in oxide for electrons, tunneling leakage limit in NMOS occurs earlier than in PMOS [4]. Besides, the tunneling probability for electrons is higher given their smaller effective mass, as compared to holes.

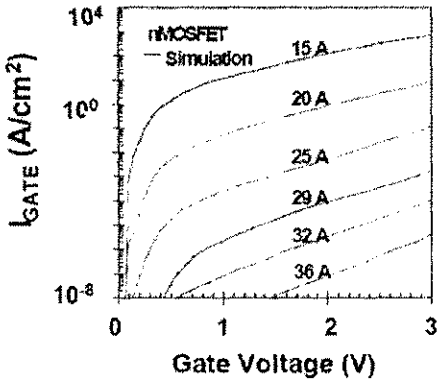


Figure 5: Gate leakage versus gate voltage for various thicknesses [7].

For thicknesses below 15 $\dot{A}$, we observe from Fig. 5 that leakage current density is high even at 1 V. Paper by Chenming Hu [8] states that static logic circuits can tolerate high leakage current density, i.e., as high as 1 A/cm^2. For 1 V operation, they have found the scaling limit to be about 2 nm. It is reported that DRAMs tolerate less oxide leakage; hence, 3 nm may be the gate oxide scaling thickness limit.

Stress induced leakage is another phenomenon where high fields stress on thin oxide generates low-field leakage through neutral oxide traps. Even at low voltages, electric fields increase when the gate oxide thickness is scaled down, this is given in the equation below as:

$$F_{ox} = \frac{V_{ox}}{T_{ox}} \tag{2.4}$$

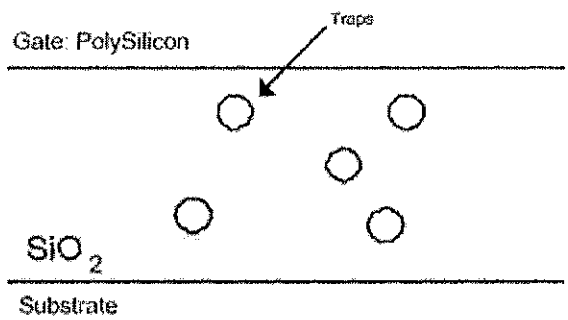
Therefore, high fields facilitate electron tunneling and tunneling leakage current makes non-volatile memories oxide scaling below 8 nm difficult.

2.1.5 Oxide Breakdown

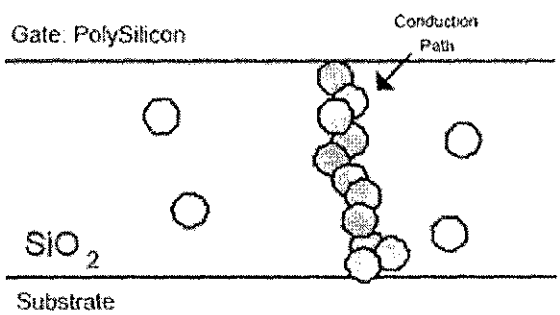
Oxide breakdown is an event that can be caused due to buildup of traps in the oxide bulk. Though other mechanisms and pathways are possible, we begin by discussing trap-related processes. The concentration of defects increases up to a critical value and sets up a percolation path between the gate and the substrate through the oxide causing the breakdown. Breakdown is

believed to be an intrinsic effect and is not due to preexisting conditions, extrinsic effects, or processing errors [8].

The evolutionary process towards breakdown and device failure at the gate oxide is shown schematically in Fig.6 (a)-(d). As seen in Fig. 6, the traps are initially non-overlapping and hence do not conduct. At high fields when more traps start to develop; a conduction channel is created from the gate to the substrate as shown in Fig. 6(b). This phenomenon leads to increased conduction in gate oxide and is called soft breakdown.

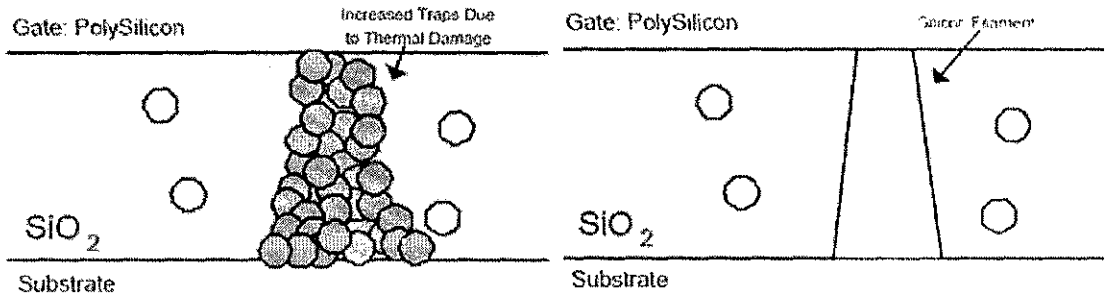


6a) Formation of traps in gate oxide.



6b) Creation of conduction paths through traps in gate oxide.

Over time, due to further and continued thermal damage, more traps are created as shown in Fig. 6 (c). Such a cycle of increased conductance leading to increased heat causes thermal runaway. This creates a lateral propagation of conduction from the breakdown spot. This process is termed as hard breakdown (Fig. 6(d)).



c) Increased traps in gate oxide after conduction d) Cross section of gate oxide after breakdown

Figure 6: Breakdown process in oxide (a)-(d) [9].

The data in Fig. 7 below predicts the oxide lifetime described a hole injection model.

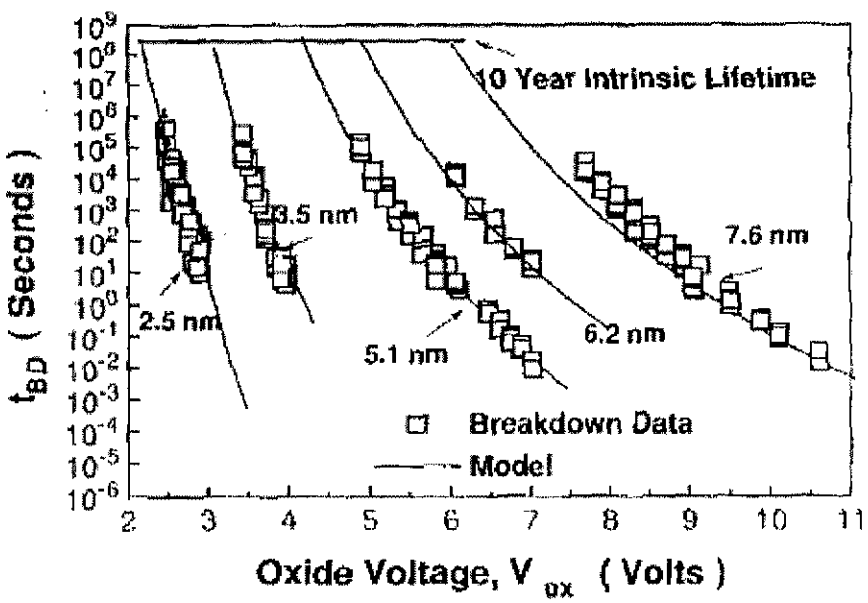


Figure 7: Oxide life time by hole injection model [8].

As shown in Fig. 7, the life time of an oxide is a function of both the gate oxide thickness (t_{ox}) and the gate voltage (V_{ox}). As the thickness of the gate oxide is reduced, the life time of the oxide decreases at a fixed voltage due to increases in electric fields.

Other factors influencing the scaling limit are transistor current and speed. As seen in equation (3), decreasing thickness has lead to the increase in MOSFET drain current. This increase in drain current, although desirable in transistor operation, occurs at a slower rate due to mobility reduction, ploy silicon gate depletion, and finite inversion layer thickness. Chenming Hu [8] also states that gate speed is reduced significantly due to T_{ox} reduction. Maximum speed was achieved at an oxide thickness higher than the thickness for 5 MV/cm breakdown limit.

Therefore, after careful examination of MOSFET scaling limits with respect to limiting factors such as time-dependent breakdown, defects, mobility degradation, poly gate depletion, inversion layer thickness, tunneling leakage, charge trapping, and gate delay it has been projected that traditional SiO_2 gate dielectrics will reach a fundamental scaling limit due to tunneling leakage current and reliability issues for thickness below 2 nm [7]. Hence, finding alternative solutions to oxide materials and dielectric insulators is an imperative need.

2.1.6 Ideal Requirements for Gate Oxide Materials

Finding an alternative gate material with high dielectric constants for future CMOS generations continues to be one of the most challenging problems in the continuous development of nanoelectronics [10]. Even though there are many materials with high-k values, any alternative gate dielectric materials must satisfy the following requirements to be practically used in device processing [11].

(i). It is imperative that the material has adequate band offsets with the interfacing semiconductor. The relationship between k and the average atomic number [Z] for the rare earth oxides from Lu to Ce has been investigated by Engstrom et al. [12]. In the rare earth metal series, from Ce to Lu, the number of electrons in the f-shell increases from 1 to 14, resulting in a complete shell. This change is related to an increase in "effective number of electrons" [13], relating to a change in polarizability. Extending this procedure to other metal oxides, a discontinuity was observed in the slope with La, Hf, Ta, and their neighboring elements in period six. The changes in crystallinity of some elements

increase the k-value in Ta_2O_5 and Pr_2O_3. It was found that a relation between the conduction band offset values and the ionicity, i.e., the difference (X_M - X_O) between the metal and oxygen electro-negativities of the oxide, could be expected.

(ii) The thermodynamic stability at an oxide/semiconductor interface. Using HfO2 as an example, this oxide is stable with respect to the Si substrate. The calculation of the HfSiO4 formation energy predicts that HfSi2 is stable up to 543.5 K.

(iii) Ensure an increase in the dielectric constant while maintaining control over the crystal structure and to suppress the recrystallization of a metal oxide. One method for HfO_2 has been to introduce selected dopants. For example, the dielectric constant of the monoclinic phase of HfO_2 is not superior to the amorphous phase, but the dielectric constant of the tetragonal phase of HfO_2 is known to be significantly higher. In order to obtain the tetragonal phase at room temperature it has been necessary to introduce cationic dopants in the HfO_2 matrix.

(iv) Ultimately, high-k materials require an atomically defined interface with silicon without an interfacial layer. Many studies have shown that atomic control of the interfacial structure by altering the chemical environment can dramatically improve the electronic properties of the interface to meet technological requirements [14]. Atomistic modeling has proven to be instrumental in understanding complex 'process–structure–properties' relationships, both in oxide/silicon and oxide/metal interfaces [15, 16]. Thus, *ab initio* calculations are an important tool for predicting a realistic oxide-silicon interface and electronic properties.

(v) Another important motivation for replacing SiO_2 with high-k materials is leakage current reduction. For this, accurate direct tunneling modeling is critical and necessary to understand the scaling limits and ensure that the selected materials are highly scalable and usable for many future generations of technology.

(vi). Assessment of the channel mobility and the careful study/evaluation of the various factors affecting channel mobility is another consideration. The transconductance of the MOSFET decides its gain and is proportional to hole or electron mobility (depending on device type). As MOSFET size is reduced, the fields in the channel increase and the dopant impurity levels increase. Both changes reduce the carrier mobility, and hence the transconductance. It has been found experimentally that surface phonon scattering in the high-k dielectric is the primary cause of channel electron mobility degradation by Chau et al. [17]. They also showed that a midgap metal–gate electrode can be effective in screening phonon scattering in the high- dielectric from coupling to the channel under inversion conditions, resulting in improved channel electron mobility.

(vii) The work function requirements for nMOSFETs and pMOSFETs dictate the selection of viable metal gate materials. The work function of a gate material for nMOSFETs must be near the conduction band of silicon, at 4.1–4.3 eV. The work function of a gate material for pMOSFETs must be near the valence band of silicon, at 5.0–5.2 eV. Mid gap work function metals have been examined to be implemented for both nMOSFETs and pMOSFETs, but exhibit large threshold voltages [18]. Consequently, it may be necessary to introduce two different gate metals in CMOS transistors in order to achieve a threshold voltage, V_{th}, which is sufficiently low for both the n-channel and p-channel MOSFETs. Fig. 8 below shows the work functions of metal gate candidates relative to the conduction and valence bands of silicon.

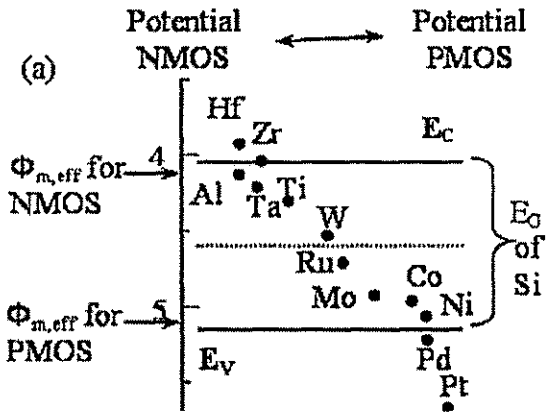


Figure 8: Work functions of various metals shown relative to the conduction and valence band edges of silicon [18].

2.1.7 Gate Stack Structures

Fig. 9 provides a schematic overview of the various regions associated with the gate stack of a CMOS transistor. The gate dielectric insulates the gate electrode from the Si bulk. Gate electrodes in modern CMOS technology are composed of poly-Si which can be highly doped and subsequently annealed in order to substantially increase conductivity. The interfaces with either the channel or the gate layer are particularly important with regard to device performance. These regions (about 5Angstroms) serve as a transition between the atoms associated with the materials in the gate electrode, gate dielectric and Si channel. Ultimately, the upper interface can be engineered in order to block boron out-diffusion from the p+ poly-Si gate electrode as well as the lower interface region must be engineered to permit low interface trap densities and minimize carrier scattering in order to obtain reliable device. With the development of oxynitride and oxide/nitride stacks, these have begun to provide a higher k-value than SiO_2 for reduced leakage.

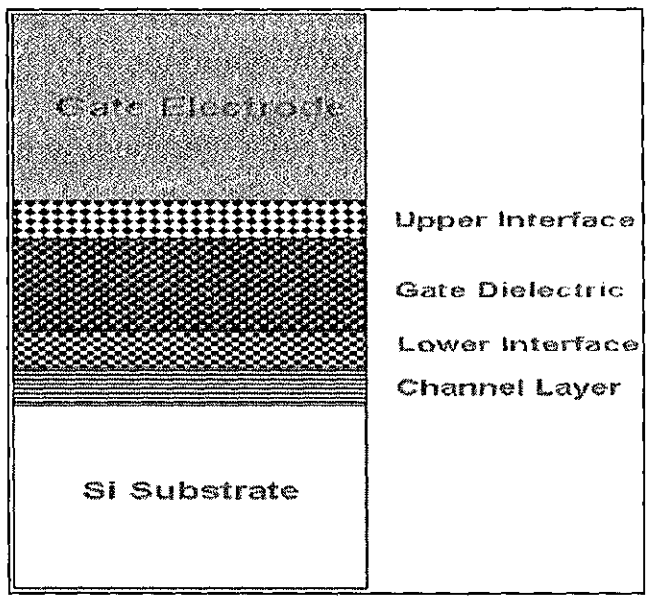


Figure 9: Schematic of a field effect transistor gate stack [19].

The need for a high-*k* dielectric as an alternative to SiO_2 was acknowledged even as early as the 1980s due to increasing gate leakage currents. However, the leakage-current problem with SiO2 gate dielectrics in the 1980s was resolved with the introduction of nitrided SiO_2 and the reduced operation voltage at the device with gate dielectric equivalent oxide thicknesses (EOTs) around 6 nm [19]. In the 1990s, interest in the high-*k* dielectric was renewed as the EOT of SiO_2 gate dielectrics scaled below 1.5 nm. From 2000 to 2003, Hf-based oxides became accepted as the leading candidates, and MOSFETs with polysilicon and TaN electrodes were successfully demonstrated at scaled equivalent-oxide-thicknesses (EOTs).

2.2 POSSIBLE MATERIALS

This scaling limit has prompted intensive basic research to find an alternative material with a higher dielectric constant (high-k) than SiO_2 to serve as gate oxides. These materials provide a physically thicker layer to suppress the quantum mechanical tunneling through the dielectric layer while achieving the needed equivalent-oxide-thickness (EOT) to enable the

continued downscaling of a wide variety of devices. The initial evaluation for gate oxides thus focused on the dielectric constants, which can be attributed to polarizability arising from electronic and ionic dipoles in the GHz frequency window that is needed for fast CMOS operation. Some of the candidate materials [20] are shown in Fig. 10 below. The fact that the dielectric response is mainly based on ionic and electronic polarization at high frequencies dictates a metal element that forms an ionic bond with oxygen and has a large atomic number (i.e., also a large number of electrons). Transition metal oxides have thus emerged as promising candidates for the insulting dielectric layer.

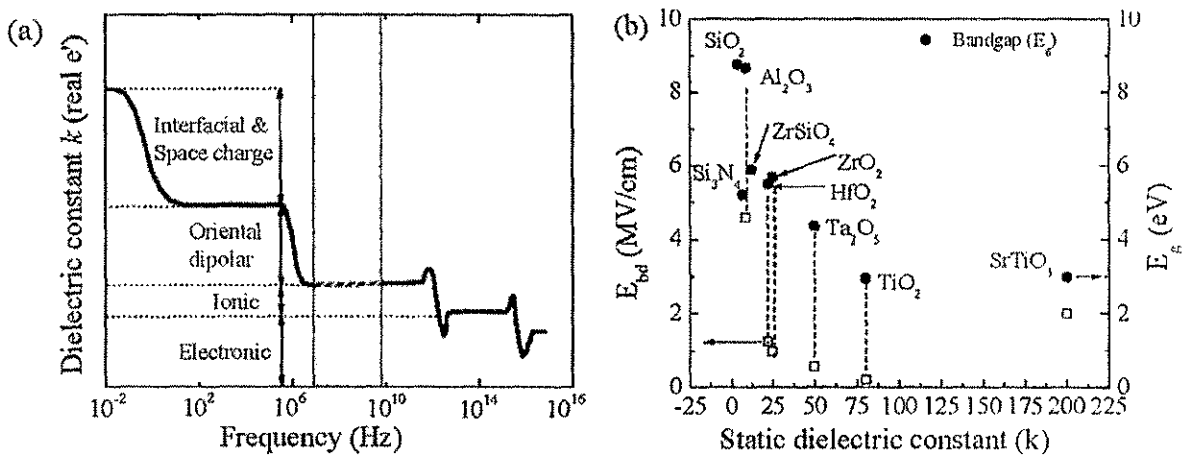


Figure 10: (a) A schematic diagram illustrating the dependence of static dielectric constant on frequency. (b) Bandgap (Eg) versus static dielectric constant (k) and electrical breakdown field (Ebd) for representative high-k materials [20].

However, it was realized that a general compromising relationship exists for these materials between the static dielectric constant (k), the attainable bandgap (E_g), and the electrical breakdown field (E_{bd}), as shown in Fig. 10 above. This behavior is expected qualitatively since stronger polarizability implies weaker bonding, and weaker bonding implies a smaller separation between bonding and antibonding energies [21]. This renders some very high-k materials, such as

$SrTiO_3$ (k = 200, E_g = 3 eV and E_{bd} = 2.2–2.3 eV), unsuitable for MOSFET applications due to their rather small bandgaps. In general, a promising high-k material should have a dielectric constant between 10 and 30, a bandgap above 5 eV, and band offsets with a semiconductor substrate above 1 eV to minimize carrier injection. High-k materials should be thermally stable within the thermal budget, i.e., up to 1000 K and 90 s, in order to form a compatible electrical interface with semiconductor substrates [22]. This consideration makes most of early high-k candidates from memory applications such as Ta_2O_5 non-ideal due to their deleterious reactions with silicon [23].

Hafnium based materials emerged over the last decade as the designated dielectrics for future generation of nano-electronics and was successfully introduced into production in 2007, as shown in Fig. 2 of [24]. Hafnium dioxide has a high permittivity (a dielectric constant about 25 and a relatively large bandgap, 5.7 eV), large heat of formation (~271 kcal/mol, higher than that of SiO_2: ~218 kcal/mol), good thermal and chemical stability on silicon, large barrier heights at interfaces with Si, and adequate compatibility with n+ polysilicon gate electrodes. At an operation voltage of 1.0–1.5 V, the leakage current through HfO_2 dielectric films was reported to be several orders of magnitude lower than that of SiO_2 with the same equivalent oxide thickness (EOT) in the 0.9–2 nm range [25, 26]. The equivalent oxide thickness (EOT) is discussed in detail later in section 2.5.

2.3 CURRENT COLLAPSE -- PHENOMENA RELATED TO TRAPPING

Current collapse is a phenomena that was first reported in GaAs-based high mobility electron transistors (HEMTs) under both DC [27] and radio-frequency [28] conditions. It has also been has been observed in GaN HMET devices that form the core of higher power and high frequency applications. GaN is a wide band gap material with high breakdown voltages and excellent transport properties. They also have superior thermal properties which resulted in the realization of heterostructure field effect transistors (HFET) in the field of lasers, heterojunction

bipolar transistors, and HEMT [29]. Heterojunction is a junction formed by two dissimilar semiconductors with different band gaps, dielectric permittivity, work functions and electron affinity. A combination of multiple heterojunctions may be called heterostructures.

Current collapse is the reduction of drain current due to carriers being trapped after the drain voltage has exceeded a certain threshold [29]. Thus, traps play an important part in determining the electrical characteristics of semiconductor devices. Also, the electric field at the gate edge and the trap density strongly affect the current collapse phenomena. This was experimentally observed in I-V characteristics of HFET. Simulations suggest that kink effect can be explained by electron trapping into barrier traps and a subsequent electron emission once a certain value of electric-field is reached. Islam & Webster [29] state that after illumination these devices restore the current that would be expected in the absence of trapping. Hashizume et al. [30] studied the passivation effects of current collapse in insulated gate AlGaN/GaN HFET using ultra-thin Al_2O_3 dielectric. Al_2O_3 is a wide band gap material with a higher dielectric constant (ε~ 9). It was reported that using an Al_2O_3 based surface passivation scheme led to no current collapse under drain or gate stress. This indicates a reliability improvement of AlGaN/GaN HEFTs with the use of high-k materials. It has also been reported [31] that edge dislocations are related to the electron trapping center and must be reduced to suppress the current collapse phenomena.

2.4 MIM (METAL-INSULATOR-METAL) STRUCTURES

2.4.1 Introduction

In section 2.1, we discussed in detail the scaling on MOSFETs which is a primary component in integrated circuits (ICs). But in order to utilize higher packing density in each chip, at the nano-scale we would have to consider scaling other components in the chip. One of the four fundamental components in an IC apart from the MOSFET is MIM capacitors and is a critical component in electronic circuits. Nanocapacitors find application in low field, high bandwidth,

real time applications such as biochemically powered telemetry nanocircuits and quantum charge pumps, high sensitivity proximity sensors, motion detectors and actuators for nanoelectronic circuits. MIM diode can also be used for solar energy conversion [32].

2.4.2 Design and fabrication of nanocapcitors

A radial parallel plate (RPP) capacitor setup is shown in Fig. 11 below, to present the effect of materials on nanocapacitor structures.

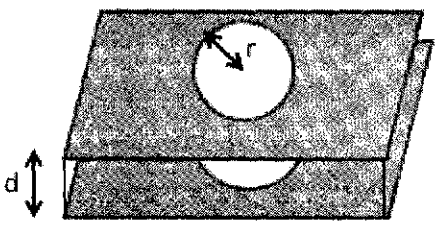


Figure 11: RPP Capacitor set up.

The RPP capacitors have two metal electrodes separated by a thin film of dielectric whose capacitance is given in equation (2.1). These structures can be developed using atomic layer deposition and other recently developed nanolithography techniques. ALD is considered as one deposition method with greatest potential for producing very thin composition of films at the atomic level. ALD is an advanced process for depositing ultrathin films one atomic layer at a time. It offers control of thickness, uniformity, quality and material properties of monolayer films that are very thin. One of the features of ALD technology that distinguishes it from other deposition techniques, is its self-limiting nature (the amount of film material deposited in each reaction cycle is constant). Entire surface is reacted to completion, disallowing further reaction to take place. This method of fabrication provided excellent conformity and the ability to produce sharp interfaces.

2.4.3 Material Permittivity

In nanocapacitors, the only parameter to increase the capacitance is the dielectric constant, given reduction in thickness leads to high leakage currents. Several solid state insulators are potential high-k dielectrics with a few of them being wide band gap materials allowing operation at higher electric fields and reducing leakage currents due to thermionic emission or tunneling. For an RPP design, Ekanayake *et al.* [32] reported the effect of dielectric constant on capacitance for materials like SiO_2, $Al2O_3$, Ta_2O_5 and TiO_2.

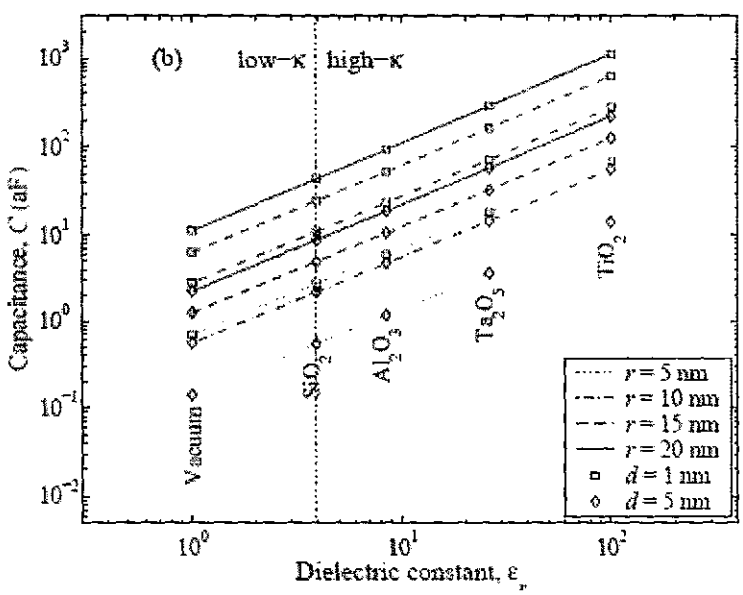


Figure 12: Capacitance versus dielectric constant [32].

As expected Fig. 12 shows an increase in capacitance with use of high-k materials. The choice of dielectric material depends on the application, electrical stability which depends on the purity and material properties of both dielectric and contact regions.

2.5 HIGH-k MATERIALS

2.5.1 Introduction

In the research for high-k materials as an alternative to SiO_2 as a gate dielectric, a more recent approach is to increase the physical thickness of the film to reduce the tunneling currents while also obtaining higher values of gate capacitance.

$$C_{ox} = \frac{k_{ox}\varepsilon_o}{t_{ox}} = C_{high-k} = \frac{k_{high-k}\varepsilon_o}{t_{high-k}}, \tag{2.5}$$

and, $$t_{high-k} = \frac{k_{high-k}}{K_{ox}} t_{ox} \tag{2.6}$$

Equation (2.6) can also be represented in terms of equivalent oxide thickness (EOT) as given in equation (2.7), which is defined as thickness of a pure SiO_2 layer which provides the same gate capacitance as a high-k layer.

$$\text{EOT} = t_{ox} = \frac{k_{ox}}{k_{high-k}} t_{high-k} \tag{2.7}$$

The International Technology Roadmap for Semiconductors (ITRS) requires continued downscaling with the equivalent oxide thickness of storage capacitors reaching to about 0.4 nm by 2011 [33]. The initial electronics roadmap required a dielectric with equivalent oxide thickness (EOT) of less than 1 nm by 2006-2007 with the following characteristics: (a) high quality interface to silicon, (b) low leakage, (c) compatibility with subsequent processing steps, and (d) long-term reliability.

In this regard, many high-k materials that consist of oxides and alloys of d-electron transition metals have been proposed as possible replacements for SiO_2. Transition metal oxides include: column III B materials such Y_2O_3 and La_2O_3; column IV B materials such as ZrO_2 and HfO_2; and column V B materials such as Ta_2O_5. Among the high-k gate dielectrics, ZrO_2 and HfO_2 have attracted much attention, due to their large band offsets and band gaps, and superior thermal stability.

2.5.2 Challenges for High-k Technology

Materials and processing related issues: The high-k substrate interface is of very high importance as it affects the overall EOT of the gate and electrical properties of the MOSFETs. The formation of interfacial layers lowers the effective dielectric constant and causes degraded electrical performance. Apart from interface issues giving rise to high defect densities, the thermal stability of the bulk of the material is also important. HfO_2 and ZrO_2 were thermodynamically stable on Si rather than TiO_2 or Ta_2O_5. After research, HfO_2 was locked in due to its more stable interface with Si than ZrO_2 and further used silicate or nitridation to stabilize the interface.

(a) Charge trapping and mobility degradation

It is reported that channel mobility in high-k dielectrics are lower compared to SiO_2. Degraded channel mobility to Coulomb scattering by oxide charge and interface traps are higher in MOSFETs with high-k dielectrics than their SiO_2 counterparts [8].

Despite significant research, the current transport mechanisms in HfO_2 based devices and stacks are not completely understood. Although tunneling leakage currents are reduced due to increase in physical thickness, process induced electrically active defect located in HfO_2 region enhance leakage currents. This brings us to examine current transport in these materials.

2.5.3 Current Transport

The model of current transport in high-k materials considers direct tunneling, tunneling via deep traps present in insulator, and trap assisted tunneling. The exchange of free carriers between the traps and the metals on the two sides of the MIM structure and between the traps and the conduction and valence bands by thermal generation and recombination many process (shown in Fig. 13).

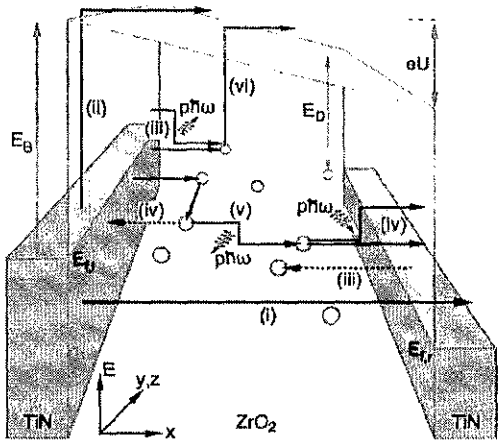


Figure 13: Transport mechanism in MIM structures [34].

1. Direct/Fowler–Nordheim (F-N) tunneling

   Recall that tunneling leakage currents was discussed in section 2.1 as one of the limiting factors in SiO_2 scaling. Direct tunneling occurs in thinner oxides and at lower fields. F-N tunneling is a special case of direct tunneling where electrons do not tunnel directly to the other side of the barrier. They tunnel from the silicon inversion layer to the conduction band of the SiO2 layer from where they are transported to the gate contact. This mechanism is more dominant for thicker dielectrics and higher electric fields.

2. Thermionic emission

   This process occurs due to heat induced flow of charge carriers from a surface over the potential barrier. The thermal energy of the electrons/charge carriers has to be greater than the work function or the potential barrier.

3. Elastic/inelastic tunneling into traps

   Electrons from the left electrode in Fig. 13 can tunnel into traps either elastically or inelastically through multiphonon transitions. The strength of the inelastic process is relatively weak since it involves intermediate virtual energy states following phonon emission/absorption transitions.

4. Elastic/inelastic tunneling out of traps

   Similarly, detrapping of electrons from trap can occur through multiphonon transitions.

5. Trap-to-trap-tunneling

   Trap assisted tunneling occurs when the electric field across the dielectric layers are increasing. High field stress gives rise to traps/defects leading to tunneling currents even at low fields. The modeling for this process has many approaches. One model is to include single traps. For each trap positions, tunneling of electrons from left electrode (cathode) to trap and from trap to anode is considered. This approach works well for slightly degraded devices and devices with thin gate dielectrics.

6. Poole-Frenkel emission

   Poole-Frenkel (PF) effect occurs at high electric fields when electrons in traps move into the conduction band of the anode. In this process, the energy barrier to electron outflow from the trap is reduced by the band-lowering due to the externally applied electric field. This induces enhanced emission into the conduction band from the traps.

From the standpoint of leakage current modeling, there have been many studies and reports in the literature [35, 36]. Of these, one recent report by Gunther *et al.* [34] discusses the above mechanisms in ZrO_2, as it was assumed that Poole-Frenkel emission from traps is the most dominant process. Further investigation into charge transport was required as good fits to experiments was achieved by using unrealistic values for material parameters in the model such as the optical permittivity. The picture of charge transport is incomplete because only charge emission from traps to anode is described while injection of carriers from cathode to traps is neglected. Therefore, in this research we study the conduction mechanisms to include injection of carriers to traps and propose a complete transport model by using HfO_2 as an example for concreteness.

CHAPTER 3

METHODOLOGY

3.1 INTRODUCTION

This chapter covers the methodology and steps undertaken to investigate the current transport through a high-k dielectric oxide. The different mechanisms and physical processes governing the transport relations in MIM structures can only be understood by setting up a numerical simulation scheme based on the steps outlined in this chapter.

Section 3.2 details the quantum mechanical models that wrap the transition rates for different transport mechanisms discussed in chapter 2. Section 3.3 deals with the assumptions made in our model and describe the effects of space charge to provide the justification and grounds for ignoring it in our model. Section 3.4 describes how the trap levels were modeled and parameters that were used in our simulation for the high-k dielectric oxide material. Finally, section 3.5 describes a software program and the set up that could be used to obtain the electrical properties of HfO_2 such as the band gap, density of states, and dielectric constant.

3.2 TRANSPORT PROCESSES

Details of the model-based transition rates for electronic flow for various processes are described next in the context to the energy band diagram of Fig. 13 already given in chapter 2. The Fermi level at the cathode (left electrode) is set to zero for reference.

Modeling details for a series of electronic transport processes in the high-k dielectric oxide follow. Brief descriptive synopsis and the inherent physical phenomena are given for each.

(i) **Electron Tunneling**: This is a phenomenon where carriers tunnel through a classically forbidden energy state or barrier. The related tunneling current density (J) in semiconductors is modeled by the Tsu-Esaki formula [37].

$$J = \frac{4\pi m_{eff} q}{h^3} \int_0^{\infty} P(E_t) N(E_t)\, dE_t \,, \tag{3.1}$$

where m_{eff} the effective mass of carrier in the material, h is the Planck's constant, $P(E_t)$ the transmission coefficient for electrons with transversal energy E_t, and $N(E_t)$ is the supply function (or energy-dependent density of states).

The transmission coefficient for electrons with transversal energy is calculated from the semi-classical method known as Wentzel–Kramers–Brillouin (WKB) approximation that was developed to solve Schrodinger's equation for the wave function in real world problems for which simple analytical solutions do not exist. The transmission coefficient for electrons will be derived later in this chapter when the two cases of direct-tunneling and F-N tunneling are discussed.

The supply function describes the difference in the supply of carriers at the interfaces of the dielectric layer [38] and is given by equation (3.2)

$$N(E_t) = \int_0^{\infty}\big((f_1(E) - f_2(E)\big)dE_p\,, \tag{3.2}$$

where E is the total energy split into E_p, the longitudinal part and E_t the transversal energy. Evaluating equation (3.2) analytically and using the Fermi-Dirac distribution the total supply function takes the form given below in equation (3.3) with V_A being the applied bias:

$$N(E) = k_B \mathrm{T} \ln\left(\frac{1+\exp(\frac{-E}{k_B T})}{1+\exp\left(\frac{-qV_A-E}{k_B T}\right)}\right). \tag{3.3}$$

Based on the magnitude of electric field, two types of tunneling can occur; direct tunneling and Fowler–Nordheim (F-N) tunneling.

a) Direct tunneling as described in the previous chapter occurs in thinner oxides and at lower fields.

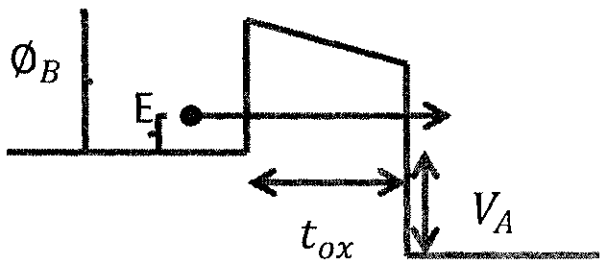


Figure 14: Energy band diagram with direct tunneling mechanism.

In direct tunneling electrons tunnel through the entire oxide and the direct tunneling rate (R_{DT}) for electrons of energy E moving from the cathode (left) in Fig. 13 and 14 can be derived from the Tsu-Esaki formula (equation 3.1) using $R_T = J * A/q$, where A is the cross-sectional area of the capacitor. Thus, R_T becomes:

$$R_{DT} = \frac{Am_{eff}k_BT}{2\pi^2\hbar^3}\int_0^\infty P(E)\ln\left(\frac{1+\exp(\frac{-E}{k_BT})}{1+\exp(\frac{-qV_A-E}{k_BT})}\right)dE\,. \tag{3.4}$$

Transmission coefficient P(E) for electrons using the WKB approximation is given by:

$$P(E) = e^{-2\int_{x1}^{x2} K\,dx}\,, \tag{3.5}$$

where $K = \frac{\sqrt{2*m_{eff}\{U(x)-E\}}}{\hbar}$, $U(x) = (q\emptyset_B - q\,F\,x)$, $x1$ and $x2$ represent the classical turning points, $\emptyset_B$ the barrier height in eV, F is the electric field and E is the energy of the tunneling electron, as displayed in Fig. 14.

For direct tunneling it is required that: $\emptyset_B - Ft_{ox} - E > 0$; $x1 = 0$ and $x2 = t_{ox}$

Using the above conditions in equation 3.5 and evaluating the integral, one gets:

$$P(E)=exp\left(\frac{-4\sqrt{2m_{eff}}}{3\hbar qF}\left\{(q\emptyset_B - qE)^{\frac{3}{2}} - (q\emptyset_B - qFt_{ox} - Eq)^{3/2}\right\}\right)\,. \tag{3.6}$$

where k_B is the Boltzmann constant, T the absolute temperature, q the electronic charge and t_{ox} the oxide thickness.

b) Similarly, for F-N tunneling the requirement is: $(\emptyset_B - Ft_{ox} - E) < 0$. From Fig. 15 we observe that $x1 = 0$ and $x2 = \frac{\emptyset_B}{E}$. Evaluating (3.5) with these conditions yields the following tunneling probability

$$P(E):P(E)=exp\left(\frac{-4\sqrt{2m}}{3\hbar qF}\left\{(q\emptyset_B - qE)^{\frac{3}{2}}\right\}\right) , \tag{3.7}$$

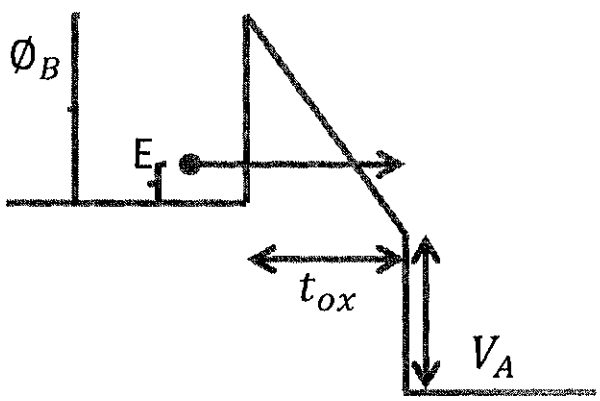


Figure 15: Energy band diagram with F-N tunneling mechanism.

and the rate R_{FN} is as given below with the $P(E)$ expression of equation(3.7):

$$R_{FN} = \frac{Am_e k_B T}{2\pi^2\hbar^3}\int_0^\infty P(E)\, ln\left(\frac{1+exp(\frac{-E}{k_B T})}{1+exp\left(\frac{-qV_A-E}{k_B T}\right)}\right)dE . \tag{3.8}$$

(ii) **Trap Assisted Tunneling (TAT)**: This is a conduction mechanism that operates in the presence of traps within the oxide. The occurrence of traps is a phenomena that can be associated with deviations in periodicity in a crystal as might arise due to the presence of defects, dislocations, or substitutional impurities. As a result of such trap levels, one can have elastic transitions of electrons with energy E from the cathode to the far anode that involve an intermediate trap state located anywhere in the oxide. In

Fig. 16, the ionization energy of a trap is denoted by u_T in electron-Volts (eV) below the oxide conduction band edge of the cathode.

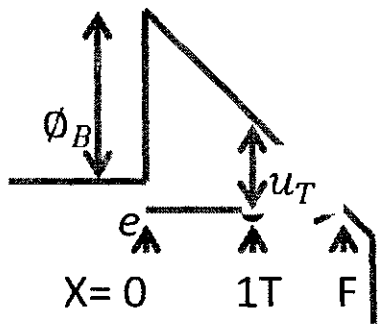


Figure 16: Energy band diagram for Trap Assisted Tunneling mechanism.

The expression for current density J_{TAT} from previous work reported in the literature [39, 40] works out to be:

$$J_{TAT} = \sum \frac{q}{exp\left(\frac{Eq}{k_B T}\right)+1} \frac{m_e (k_B T)^2}{2\pi^2 \hbar^3} \frac{P1\, P2}{P1+P2}, \tag{3.9}$$

where the term $\left[exp\left(\frac{E}{k_B T}\right) + 1\right]$ accounts for electron probability at the injecting electrode, while the factors $P1$ and $P1$ are

$$P1 = exp[-2\int_0^{x_{1T}} k(x)dx] \quad , \tag{3.10}$$

$$P2 = exp[-2\int_{x_{1T}}^{x_F} k(x)dx] \quad , \tag{3.11}$$

x_{1T} Longitudinal location of the defect site ,

and $k(x) = \sqrt{(\frac{2m_e}{\hbar^2})q(\emptyset_B - Fx - E)}$ is the wave vector.

Expressions 16a and 16b can be evaluated for the following conditions. The upper limit x_F either equals t_{ox} if the field F is low $[F < u_T/(t_{ox} - x_{1T})]$, or $x_F = x_{1T} + u_T/F$ at higher electric fields [i.e., $F < u_T/(t_{ox} - x_{1T})$]. In either case (low or high F values), the expression for $P1$ evaluates to:

$$P1(E) = exp\left(\frac{-4\sqrt{2m_e}}{3\hbar F}\left\{(Fx_{1T} + u_T)^{\frac{3}{2}} - u_T{}^{3/2}\right\}\right) \quad . \tag{3.12}$$

The expressions for $P2(E)$, for the low and high field regimes are respectively, are given as:

$$P2(E) = exp\left(\frac{-4\sqrt{2m_e}}{3\hbar F}\left\{(u_T)^{\frac{3}{2}} - \{u_T - F(t_{ox} - x_{1T})\}^{3/2}\right\}\right). \tag{3.13}$$

and $$P2(E) = exp\left(\frac{-4\sqrt{2m_e}}{3\hbar F}\left\{(u_T)^{\frac{3}{2}}\right\}\right). \tag{3.14}$$

As before the rate R_{TAT} is related to the current density by $J_{TAT} = R_{TAT}\,(q/A)$.

(iii) **Multiphonon Emission and Absorption**: In addition to the trap assisted tunneling mechanism, Hermann and Schenk [41] discuss the transport via multiphonon transitions. This current is calculated by adding the contributions of inelastic electronic transitions between the electrode and defects that form multiple percolation paths through the oxide.

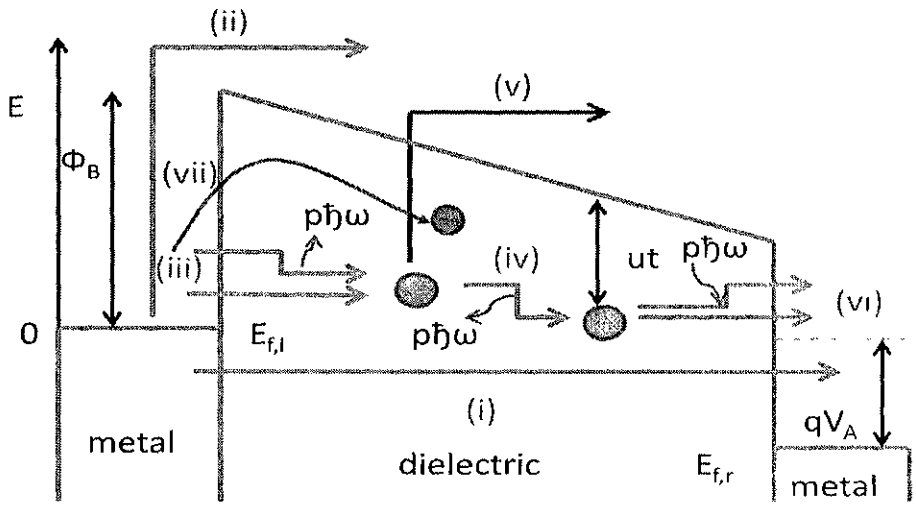


Figure 17: Energy band diagram for multiphonon emission & absorption.

This leads to electronic transfers assisted by multiphonon transitions (pħω) as shown in Fig. 17. Electrons from the cathode travel to the trap site via inelastic multi-phonon emission and from the trap to the anode via multi-phonon absorption. The multi-phonon emission rate R_{EM} and the multi-phonon absorption rate R_{ABS} can be evaluated by using equations 14, 16, 18, 19, 20, 22, and 24 as presented in detail in Ref. 41. The expressions turn out to be:

$$R_{EM} = \sum_m \frac{2^{3.5} m_e^{\frac{3}{2}} T_l(E_m,x) r_D^3 q^{2.5} F^2 \sqrt{\emptyset_B - Fx - u_T + m\hbar\omega}\, L_m(z)}{m_{cox} h^2 E_{gox} \left[exp\left(\frac{\emptyset_B - Fx - u_T + m\hbar\omega}{kT}\right) + 1\right]}, \quad (3.15)$$

$$R_{ABS} = \sum_m \frac{2^{3.5} m_e^{\frac{3}{2}} T_r(E_m,x) r_D^3 q^{2.5} F^2 \sqrt{\emptyset_B - Fx - u_T + m\hbar\omega + v_{bias}}\, L_m(z)}{m_{cox} h^2 E_{gox}\, exp\left(\frac{m\hbar\omega}{kT}\right)}, \quad (3.16)$$

where, $L_m(z) = \left[\frac{f_b+1}{f_b}\right]^{m/2} exp\left(-S\,(2f_b+1)\right) I_m(z)$ with $f_b = \left[exp\left(\frac{\hbar\omega}{kT}\right) - 1\right]^{-1}$, $Z = 2S\sqrt{f_b(f_b+1)}$, ħω is the phonon energy, $r_D = \frac{\hbar}{\sqrt{2m_{ox}\, u_T}}$ is the localization radius, and m denotes an integer. Also, in equation (3.15) above:

$$T_l(E_m,x) = exp\left(\frac{-4}{3\hbar F}\sqrt{2m_e}\left\{(Fx_{1T} + u_T - m\hbar\omega)^{\frac{3}{2}} - (u_T - m\hbar\omega)^{\frac{3}{2}}\right\}\right), \quad (3.17)$$

and, $T_r(E_m,x) = exp\left(\frac{-4}{3\hbar F}\sqrt{2mq}\left\{(u_T - m\hbar\omega)^{\frac{3}{2}} - (u_T - m\hbar\omega - F(t_{ox} - x_{1T}))^{\frac{3}{2}}\right\}\right.$

$$\left. .\, U[(u_T - m\hbar\omega - F(t_{ox} - x_{1T}))]\right) . \quad (3.18)$$

In equation (3.18), the last term $U(x)$ denotes the Heaviside step function.

(iv) **Poole Frenkel Emission**: This is another inherent process of taking trapped electrons from defect states and facilitating their transition towards the anode as depicted in Fig. 18. It is facilitated by the presence of an externally applied electric-field. Such a field effectively changes the energy bands (lowers them along the downstream direction) which helps eject the electrons from the trap towards the anode.

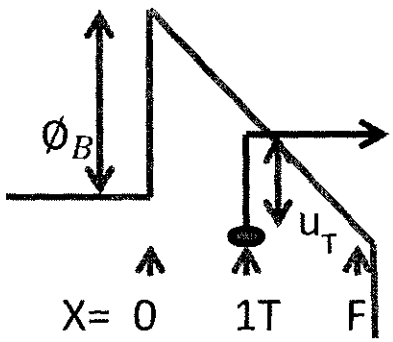


Figure 18: Energy band diagram for Poole-Frenkel.

The rate R_{PF} associated with this emission is given in [42].

$$R_{PF} = \vartheta \ exp\left[\frac{-q\,u_T}{k_B T}\right] ([1+ (\beta - 1)exp(\beta)\}/\beta^2] + 1/2) \quad , \tag{3.19}$$

where $\beta = \left[\frac{q^3 F}{\pi \varepsilon_0 \varepsilon_\infty k_B{}^2 T^2}\right]^{1/2}$, and ϑ is a typical phonon frequency (~10^{13} Hz).

(v) **Schottky Emission:** Along with Poole-Frenkel that takes out electrons from traps, the Schottky emission process is considered to inject carriers into the traps [43]. The rate from Schottky emission is calculated from current density in [57] and is given in equation (3.20).

$$R_{SCH} = \frac{A*T^2*Area}{q} * \exp\left(\frac{-q(\emptyset_B - \sqrt{\frac{qF}{4\pi\varepsilon_\infty \epsilon_0}})}{k_B T}\right) \tag{3.20}$$

where $A = \frac{4\pi q m_{ox} k_B^2}{h^3}$ = 1.2 x 10^6 *(mox/me) Amps/(m^2K^2) and T is the temperature in Kelvin.

As a result of the various transitions allowed into (and out of) the trap states, i.e. processes (ii), (iii) ,(iv) & (v), the net rate equation for the oxide trap density N_T can be written as:

$$dN_T/dt = R_{EM}\, N_T\,(1 - f_T) + R_{SCH}\, N_T\,(1 - f_T) \; - \; R_{ABS}\, N_T\, f_T \; - \; R_{PF}\, N_T\, f_T \; . \tag{3.21}$$

In steady-state, $f_T = (R_{EM} + R_{SCH})/[R_{EM} + R_{SCH} + R_{ABS} + R_{PF}]$, which yields a net current density J_{inelas} given as:

$$J_{inelas} = \{ q (R_{EM} + R_{SCH}) * (R_{ABS} + R_{PF}) N_T t_{ox} \} / [R_{EM} + R_{SCH} + R_{ABS} + R_{PF}]. \quad (3.22)$$

(vi) **Elastic Defect-to-Defect Transitions:** This process as shown in Fig. 17, depends on the energy of the traps below the conduction band. Assuming delta like potentials, the rates for elastic defect to defect transitions can be evaluated. As given in detail in Ref. [3], this is given as:

$$R_{DD} = \vartheta \, exp\left(\frac{-2 r_{DD}}{r_D}\right), \quad (3.23)$$

where $r_D = \frac{\hbar}{\sqrt{2m_{ox} u_T}}$ is the localization radius, ϑ the typical phonon frequency, and $r_{DD} = \frac{1}{N_D^{1/3}}$ with N_D being the average defect density.

(vii) **Inelastic Multiphonon Transitions**: The rate for transitions involving p number of phonons each with energy $\hbar\omega$ is given by the following expression reported in Ref. [3]:

$$R = R_{Rid} \frac{\pi}{\hbar^2 \omega} exp\left(-S (2f_b + 1) - \frac{p\hbar\omega}{2k_B T} \right), \quad (3.24)$$

where R_{Rid} is a complicated factor as discussed by Ridley [44], p is an integer, S the Huang-Rhys coupling factor (taken to equal 17 as reported in Ref. [45]), and f_b the phonon Bose-Einstein occupancy given as: $f_b = [exp\{(\hbar w_0)/(k_B T)\} - 1]^{-1}$.

From the rate equations above for different transport processes, it can be seen that they are functions of electron energy. It has been speculated that trap-assisted tunneling [46, 47] and

Poole-Frenkel (PF) emission [3] are perhaps the two most dominant transport processes in high-k dielectrics. Also, Ref. [48] suggests that bulk traps have an important role in leakage currents in the current high-k oxides than interface traps since they are spread over a larger volume. Such charge trapping requires investigation as it gives rise to a time-dependent bias instability in high-k dielectrics [49, 50].

3.3 SPACE CHARGE

Many of the transition probabilities are a function of the spatially dependent electric field, which in turn depends on the charge distribution. The charge distributions can, in principle, change as seen through the following argument. Many of the transition processes involve the electron trapping at defects. This would lead to a change in the spatial distribution of the charge within the high-k oxide. Such changes in charge would then alter the electric field. However, in our case, space charge effects due to electron trapping within the oxide were ignored based on the premise that electric field changes due to charge variations would be negligible. The following estimate of the influence of charge variation on the electric fields supports our premise.

Assuming a charge density (N_c) of ~ 10^{16} m^{-2} at the traps, the estimated deviation ΔE in electric fields associated with the space charge would roughly be ~7×10^6 V/m [$= q\, N_c\, /(\varepsilon_r \varepsilon_0)$] based on the Poisson equation, with ε_0 being the permittivity of free space and ε_r the oxide dielectric constant that is assumed to be 25 from [58] in case of HfO_2. Since the oxide thickness of interest here is in the 5-10 nm range, for voltages up to ~3 Volts, the average externally applied electric field of ~3×10^8 V/m is much larger than perturbations arising from oxide space-charge effects (7×10^6 V/m). Therefore, our uniform E-field assumption is justified.

3.4 TRAP LEVELS & PARAMETERS

The dominant transport process as discussed in previous sections, depend on the defect energies and other parameters used in our simulation. In HfO_2, electrical energy levels of different charge states of oxygen vacancy and its interstitial in HfO_2 are the primary active sites [51]. The parameter values and energy levels used in our simulation were obtained from studies conducted by several researchers as reported in Refs. [40, 45, 51-54 and 57-64]. The required parameters are tabulated in section 4.2 & 4.5. The barrier height given assumes a Cromium electrode for HfO_2 gate oxide.

3.5 CASTEP

The electrical parameters used in our simulation have been found experimentally for the high-k dielectric oxides such as HfO_2. However, these were typically materials that were available and grown by the best available techniques such as Atomic Layer Deposition (ALD). Due to the emergent nature of these materials and the relatively new and immature technology, the materials are not perfect, nor completely defect-free. In actual practice, it becomes necessary to look at the following aspects: (i) material that has inherent defects which could affect (or perturb) the electrical and other material properties, (ii) probe situations wherein defect densities might be tailored through changes in processing or alternative technologies. It is important to assess the extent of changes in processing on the parameters. For example, exposure of high-k HfO_2 material to nitrogen could passivate the traps and enhance the electrical characteristics. However, this is an aspect that can only be evaluated and predicted through numerical computations of the material properties.

The ability to probe and predict the material properties based on atomistic details of the material can be calculated from a quantum mechanics based software program called CASTEP. CASTEP employs the density functional theory plane-wave pseudopotential method, which allows you to perform first-principles quantum mechanics calculations that explore the properties

of crystals and surfaces in materials such as semiconductors, ceramics, metals, minerals, and zeolites [55]. Without experimental input, this software allows us to study band structure, density of states, optical properties, surface chemistry and structural properties of materials that exist in nature.

In order to generate chemical and physical properties of crystals and surfaces, the CASTEP module allows five different tasks (as shown in Fig. 19), we focus on the energy task and geometry optimization for obtaining band structure, density of states and the dielectric function. Some of the tasks involved in such a CASTEP calculation for evaluation of material properties are briefly discussed below.

- Single point energy calculation: This allows for the calculation of total energy of the specified 3D periodic system and its physical properties.
- Geometry optimization: This mode within CASTEP allows the user to refine the geometry of the 3D near-periodic system to obtain a stable structure

The calculation module also allows us to choose functional (approximation methods for solving density functional theory in CASTEP) as shown in Fig. 24.

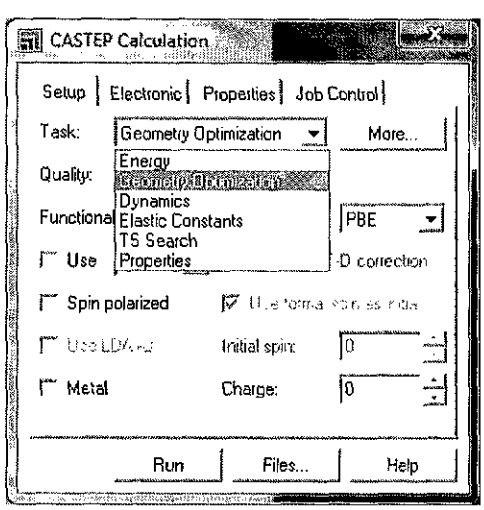


Figure 19: CASTEP task options [55].

In addition to the above tasks, the properties calculation tab allows us to restart a completed task to compute additional properties (Fig. 20) that are not calculated in the tasks mentioned above.

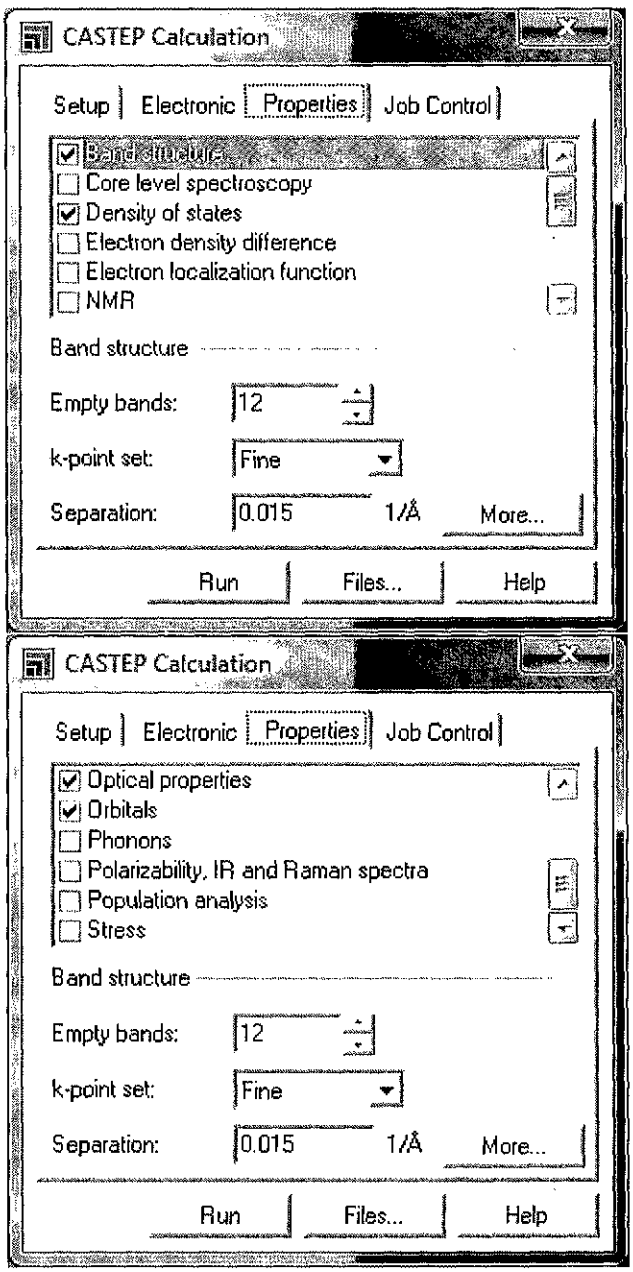


Figure 20: Properties tab in CASTEP [55].

The analysis module in the figure below (Fig. 21) provides us with an option to customize the plots/outputs for further analysis.

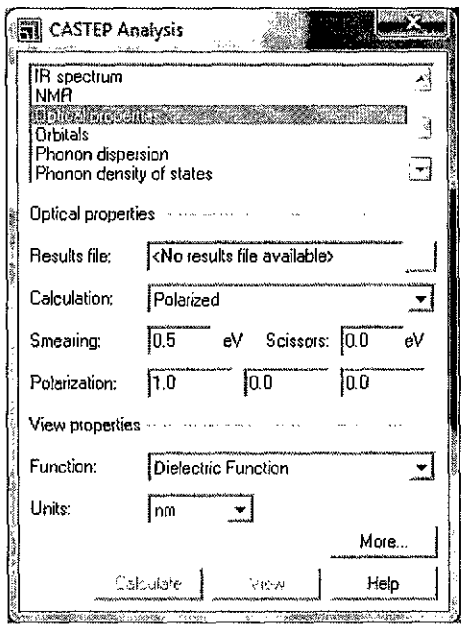


Figure 21: Analysis Module in CASTEP [55].

Using CASTEP, the HfO_2 cubic structure can be built by either importing the structure from Crystallography open data base or by using the build module (Fig. 22) in the software. In the latter case, we require prior information and knowledge of the material's space group, lattice parameters, and internal coordinates.

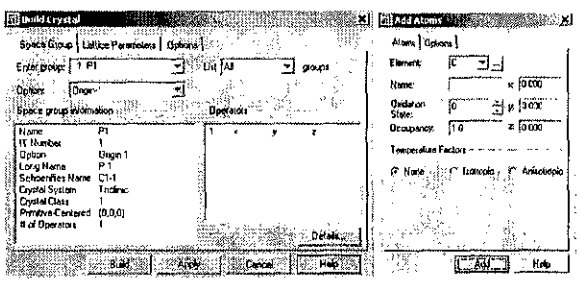


Figure 22: Build Crystal & add atoms in CASTEP [55].

In our case, the unit cell was imported from the open database, and 2 unit cells (39 atoms) were built in the software as seen in Fig. 23 where blue atoms represent hafnium and the red represent oxygen.

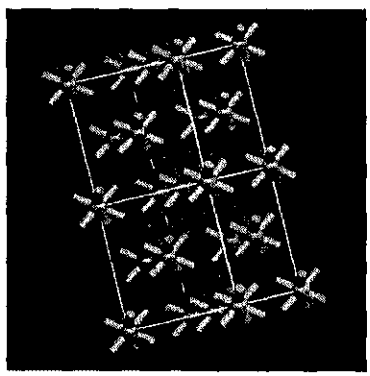


Figure 23: HfO_2 cubic structure (2 unit cells) [55].

After the oxide structure is built, the calculation module (Fig. 25) was set up to run the simulation. The most commonly used function to solve the Kohn-Sham functional (Exchange-Correlation functional) in density functional theory are the LDA (Local Density Approximation), and GGA (Gradient Corrected Approximation) for optical properties such as dielectric constants although CASTEP recommends sX-LDA (fully nonlocal Screened Exchange & LDA correlation) for better estimate of bandgap [55].

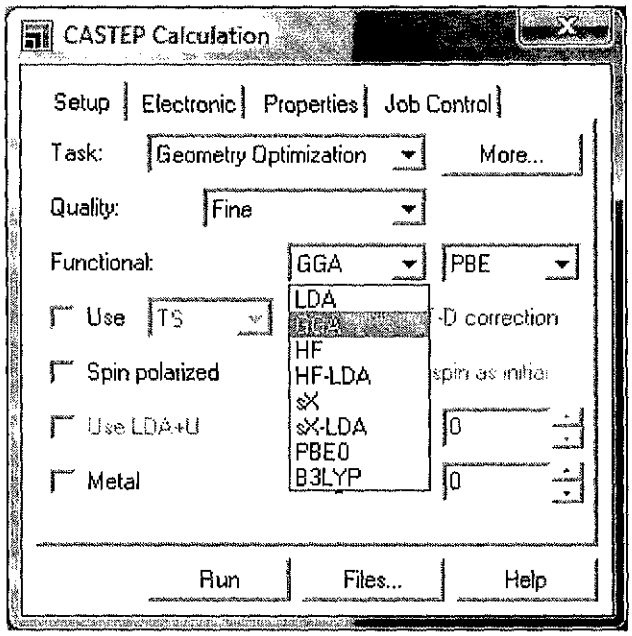


Figure 24: CASTEP functional methods [55].

The electronics tab in Fig. 25 allows us to set the quality of output through cut off energy, SCF tolerance, and k-point set options. DFT in CASTEP uses the pseudo potential method which is an approximation that replaces complicated effects of motion of non-valence electrons with effective potential. This method is effective for numerical computation as it reduces the basis set size and can further be divided as soft (Ultrasoft) and hard (Norm-Conserving) based on the degree of hardness (i.e. number of Fourier components used for accurate representation) [55]. In the case of Norm-Conserving (with higher number of Fourier components that increase the basis set size), outside of a cutoff radius, the norm of each pseudo-wave function is identical to its corresponding all-electron wave function. Therefore, for better approximation, we employed Norm-Conserving pseudo potential method in our calculations.

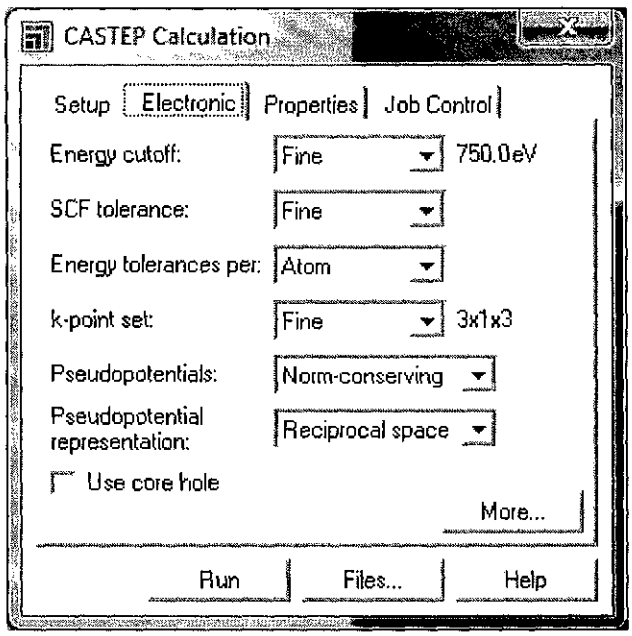


Figure 25: Electronic calculation set up tab in CASTEP [55].

As stated before, we chose to observe the band structure, density of states, and optical properties of HfO_2 cubic structure using the properties tab in CASTEP calculation module. The output from this set up is discussed in chapter 4 along with the results from our model for leakage current density.

CHAPTER 4

RESULTS AND DISCUSSION

4.1 INTRODUCTION

Numerical simulations of the transport processes described in section 3.2 were carried out using the MATLAB software tool. For the purpose of demonstration, rates from various conduction mechanisms based on their mathematical models described in chapter 3 were quantitatively determined to underscore and evaluate the role and relative significance of each process. Later in the chapter, the effects of traps on defect dependent mechanisms have been discussed. The material parameters control and form the basis for the transport processes. Hence, for completeness, the material parameters need to be determined. Towards this goal of modeling material parameters for the high-*k* dielectrics, density functional theory (DFT) was identified as the most promising and appropriate route. The DFT simulations were carried out in CASTEP to extract and validate the material parameters for HfO_2, and the results obtained are also presented in this chapter. The material parameters from CASTEP and experimental parameters reported in studies are used to simulate and validate the total leakage current density as a function of electric field and applied bias. In general, our model was constructed with an aim to estimate leakage current density and its underlying dominant transport process for high-*k* materials. Also, the alternative high-*k* material ZrO_2 was also considered, and the resulting leakage current density from our simulations is presented. Comparisons for our model validation with the experimental data published are also presented and discussed later in this chapter.

4.2 RATES FOR TRANSPORT PROCESS IN Cr/HfO_2/Cr MIM STRUCTURES

At first, all of the rates for the various conduction mechanisms in HfO_2 are analyzed based on the rate equations described in section 3.2. These calculations were carried out for a Cr/HfO_2/Cr metal-insulator-metal (MIM) structure with a gate oxide physical thickness (t_{ox}) of

10nm and an area of 1.77 mm^2 at 298 K. The applied bias in our simulation was varied from 0 V to 3 V. Other parameters and material properties of HfO_2 used in this simulation are given in Table 4.1 below. The results from this simulation, with an emphasis on the rates of the various constituent processes are discussed in this section.

Table 4.1: Parameters for HfO_2.

Parameters	**Value**	**Parameters**	**Value**
Permittivity of free space	8.854×10^{-12} F/m	Band gap	5.5 eV
Optical permittivity	4	Barrier height	1.75 eV
$\hbar$	1.054×10^{-34} m^2 kg/s	Trap energy	0.8 eV and 2.1 eV
Electronic charge	1.6×10^{-19} C	Defect density	1×10^{23} m^{-3}
Electronic mass (m_e)	9.11×10^{-31} kg	Phonon frequency	1.0×10^{13}
Electronic mass in oxide	0.15 m_e	Huang-Rhys factor	17
$\hbar\omega$ for inelastic multiphonon transitions	0.07 eV	R_{Rid}	8.0×10^{-21}
Boltzmann constant	1.38×10^{-23} m^2 kg/s^2	Number of phonons	1

(A) Direct tunneling

The rate of direct tunneling process was evaluated using equation (3.4) given in chapter 3. The results obtained are given in Fig. 26 below. As mentioned before, it is observed that the rate shows an increasing trend at the lower and moderate fields up to about 1.9 MV/cm. This is easily understood in terms of the energy-band diagram shown in Fig. 17. A requirement for direct tunneling, as stated in the context of equation (3.6) is: $\emptyset_B - Ft_{ox} - E > 0$. So, as the electric field F increases, electrons having an ever-decreasing energy can participate in the process. Consequently, the direct tunneling rate begins to

decrease for very high field. At these strengths, the oxide barrier effectively becomes triangular, and the Fowler-Nordheim process, as discussed next, begins to take over.

For thinner oxides, for example at 5nm, the rate of direct tunneling is higher as shown in Fig. 27. It may also be noted that since the oxide thickness (t_{ox}) is lower, it would take a much larger electric field to satisfy the same condition of: $\emptyset_B - Ft_{ox} - E > 0$. With the thickness ratio being 1:2, the electric field for this condition can then be expected to be around 3.8 (=2 x 1.9) MV/cm. Since the electric field is only plotted up to 3 MV/cm in Fig. 27, this maxima followed by a decreasing trend is not seen in Fig. 27 below.

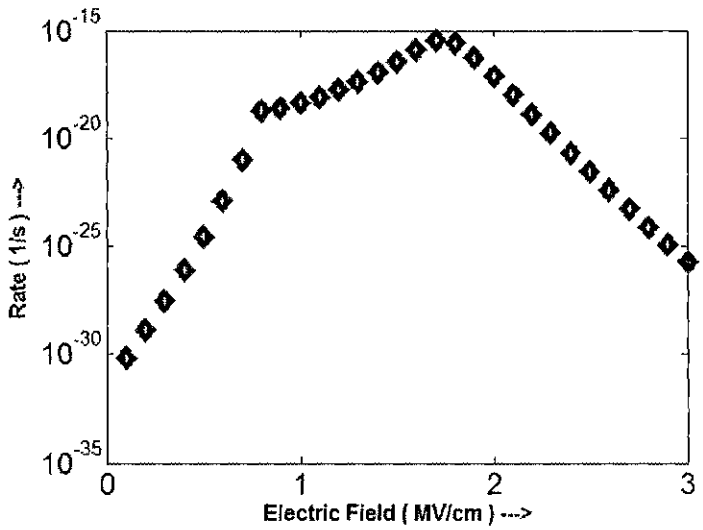


Figure 26 Direct tunneling rate, t_{ox}= 10nm.

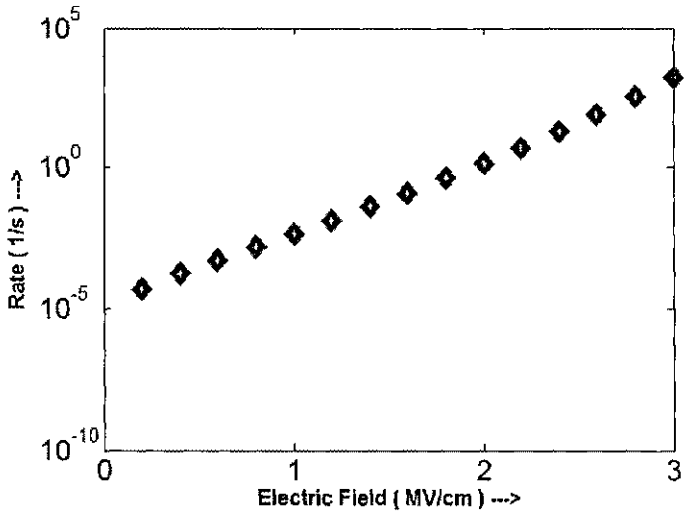


Figure 27: Direct tunneling rate, t_{ox}= 5nm.

(B) Fowler-Nordheim (FN) tunneling

The rate for Fowler-Nordheim (FN) tunneling was evaluated using equation (3.7), and the result is plotted in Fig. 28 for a 10 nm oxide thickness. In comparison with direct tunneling, this process is predominant at higher fields. In this case, the rate of FN tunneling is much higher than the rate of direct tunneling from about 1MV/cm. The higher rates are easily understood based on the inherent physics. The potential barrier becomes triangular at these high electric fields. Consequently, electrons no longer have to traverse as large a distance. Since the rates have a negative exponential dependence on distance, the FN rates increase substantially at the high fields. However, since both direct and FN tunneling rely on quantum mechanical tunneling as the basic mechanism, from this point onwards we will combine these two processes. Hence, the sum of direct and FN tunneling will be addressed as a collective process for electron tunneling, in general.

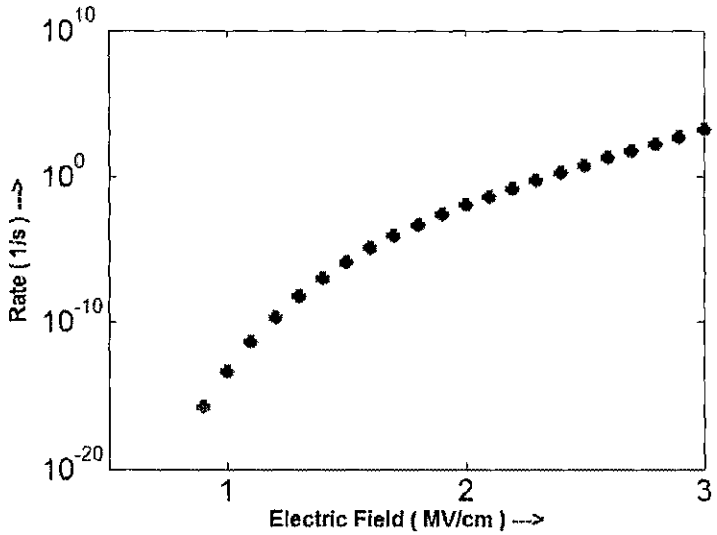


Figure 28: FN tunneling rate, t_{ox}= 10nm.

(C) Trap Assisted Tunneling (TAT)

The rate of the elastic trap assisted tunneling process (R_{TAT}) is calculated from the expression of current density (J_{TAT}) as given previously in equation (3.9). To reiterate, this relation is: $J_{TAT} = R_{TAT}\ (q/A)$. This trap dependent phenomena in HfO_2 was modeled with two uniform defect levels along the thickness of the insulator/oxide. Two defect levels were assumed based on the reported energy levels associated with the oxygen defects in HfO_2. More precisely, the electrical trap energy levels of O_2 differ since they depend on the different charge states of the oxygen molecule and/or their location which can be interstitial in nature. These energy levels could be measured, but can also be calculated using DFT techniques. From an on defect energy states in high-*k* gate oxides, it has been reported that oxygen vacancy is the main electrically active defect, and yields trap levels below the oxide conduction band [51].Analysis of the trapping data by over a wide temperature range produced two trap levels at 0.8 eV and 2.1 eV below the oxide conduction band [51]. Consequently, these values were used in our simulation to yield

the rate shown in Fig. 29 below. From Fig. 29, it becomes obvious that the current contribution from the TAT process can become sizeable at the high electric fields.

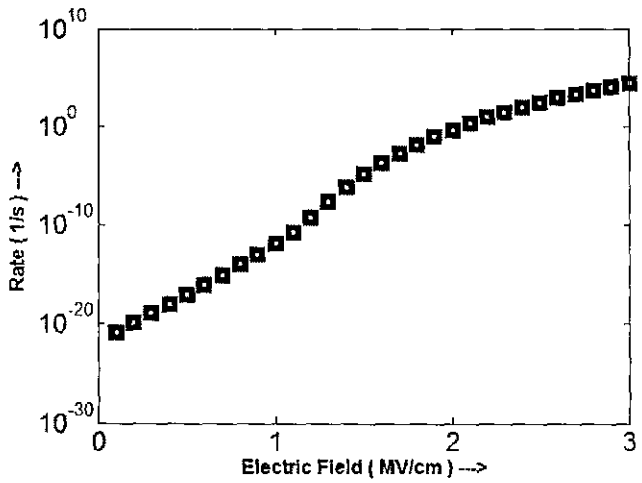


Figure 29: The trap-assisted-tunneling (TAT) rate for t_{ox}= 10nm.

(D) Inelastic Emission

The rate of electronic transitions assisted by multiphonon transitions from electrode (cathode) to the oxide traps was given by equation (3.15) in chapter 3. The result obtained numerically is plotted in Fig. 30. The values are very low and can essentially be neglected in comparison to the other current conduction processes described above. The reason for the low strength of this process is based on the multiphonon nature of this mechanism. The transition is thus not direct but instead relies on the collective participation of several phonons. Physically, this leads to several sequential processes and so slows down the overall transition rate considerably.

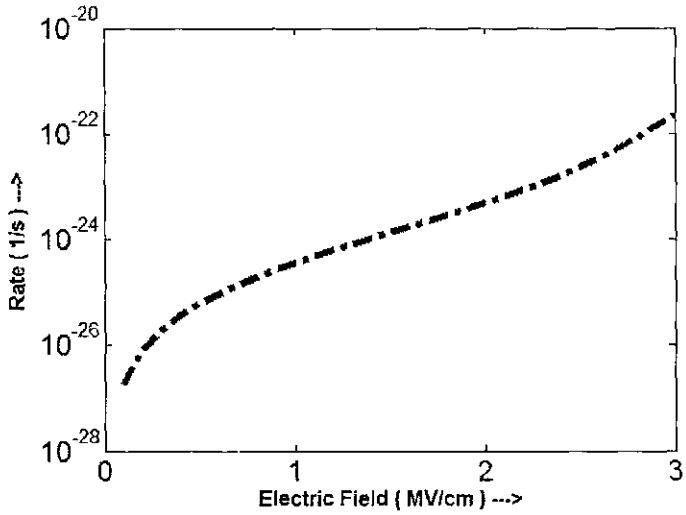


Figure 30: Inelastic emission rate for t_{ox}= 10nm.

(E) Inelastic absorption

The rate of electronic transitions assisted by multiphonon transitions from oxide traps to the anode (right electrode) is given by equation (3.16), and this rate result is plotted in Fig. 31. As with the inelastic emission which is also a multiphonon process, the inelastic absorption is again a very weak process.

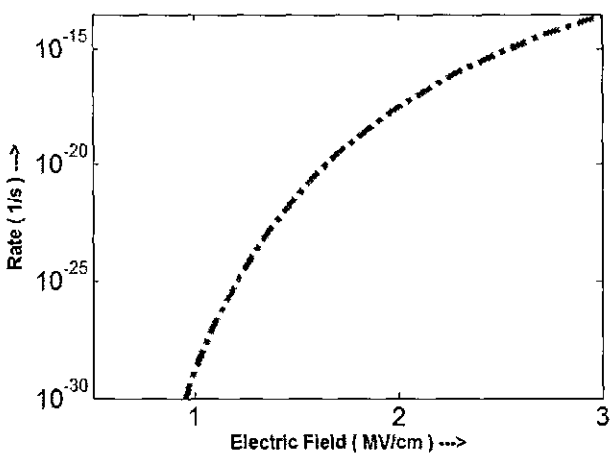


Figure 31: Inelastic absorption rate for t_{ox}= 10nm.

(F) Multiphonon Transitions

A quantum mechanical calculation of the multiphonon, non-radiative transition rate for electrons was calculated using equation (3.24), and the result is given in Fig. 32. This transition is independent of the electric field and has a rate that would be insignificant at high electric fields. However, the main role for this process would be at the low electric fields, and could influence the leakage current at low voltages. In the plot, the Ridley factor was adjusted slightly to yield the curve shown. This adjustment was done to bring the low-field current density, obtained from the rate and discussed later in this chapter, roughly in line with experimental data. This aspect is discussed in greater detail in the context of figs. 44 and 46 that will touch upon the reported experimental data.

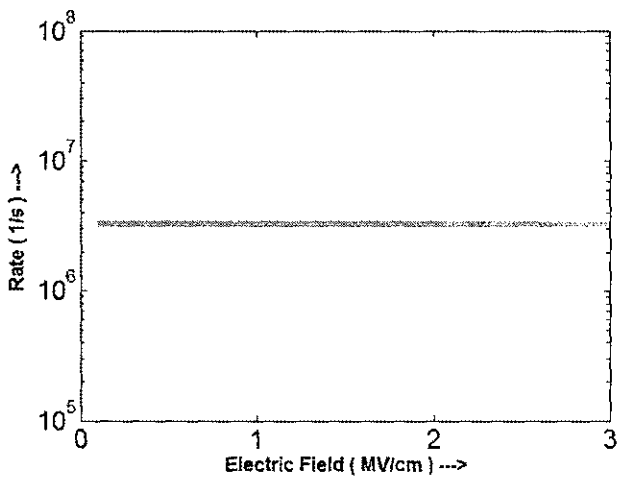


Figure 32: Multiphonon transition rate for t_{ox}= 10nm.

(G) Schottky Emission

The rate from Schottky emission process described in eqn 3.23 is given in Fig. 33. This process can be seen to have moderate to large significant in the moderately low field regime between the 1-2 MV/cm range. For higher fields, i.e., above 2 MV/cm, FN

tunneling begins to contribute significantly to leakage current (see Fig. 28) in comparison to Schottky emission.

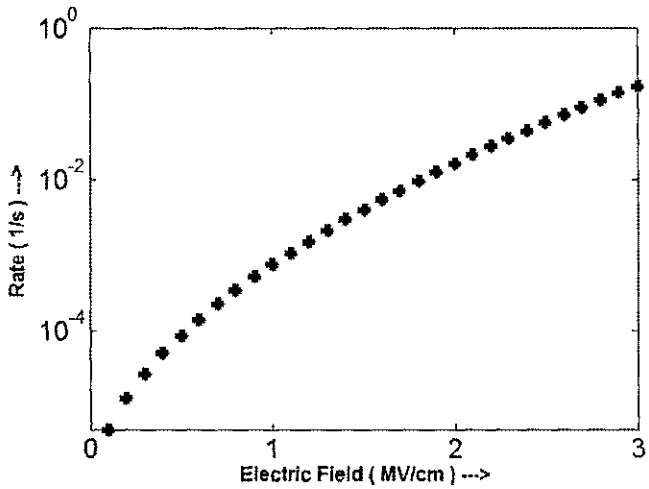


Figure 33: Schottky emission rate for t_{ox}= 10nm.

(H) Poole-Frenkel Emission

An important process that takes electrons from defects to the anode is the Poole-Frenkel mechanism, and this rate was calculated from equation (3.19). The result obtained is presented in Fig. 34.

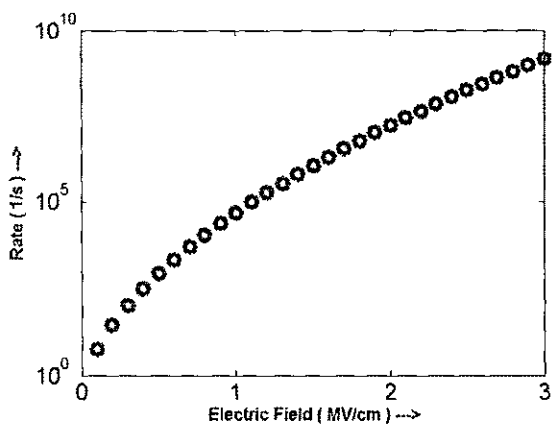


Figure 34: Poole-Frenkel rate for t_{ox}= 10nm.

As discussed in chapter 3, the various transitions that are allowed into and out of traps in oxides were modeled to set up a net rate equation for oxide trap density. The net rate obtained at steady state is given in equation (3.22). The rate for such a steady-state can then be calculated as a function of electric field. The results for fields in the range of 1-3 MV/cm were obtained, and are given in Fig. 35 below.

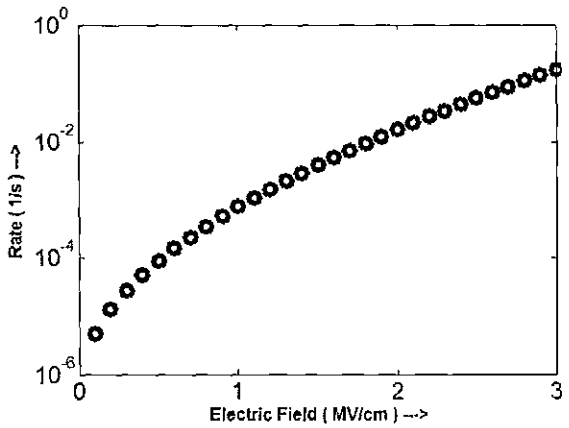


Figure 35: Total Rate (Inelastic emission, Inelastic absorption, Poole-Frenkel and Schottky).

(I) Defect to Defect (D-to-D)

The rate of defect to defect transitions in an oxide with defect density 2.5×10^{22} m^{-3} and uniform defect states due to oxygen vacancy at trap levels 0.8 eV and 2.1 eV below the oxide conduction band was calculated since these are some of the typical values reported for HfO_2. The result for the rate obtained is shown in Fig. 36.

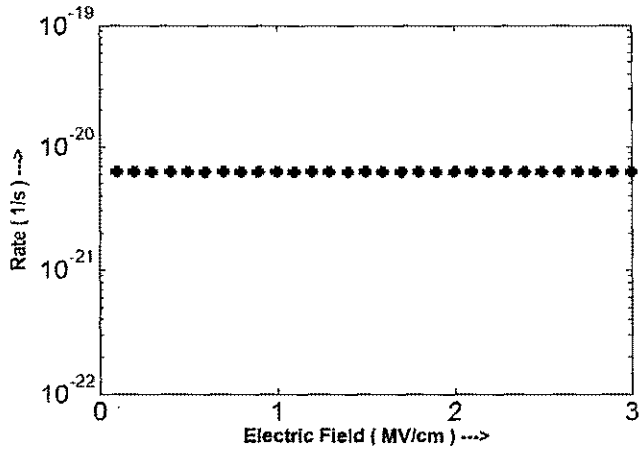


Figure 36: Defect to defect rate for t_{ox}= 10nm.

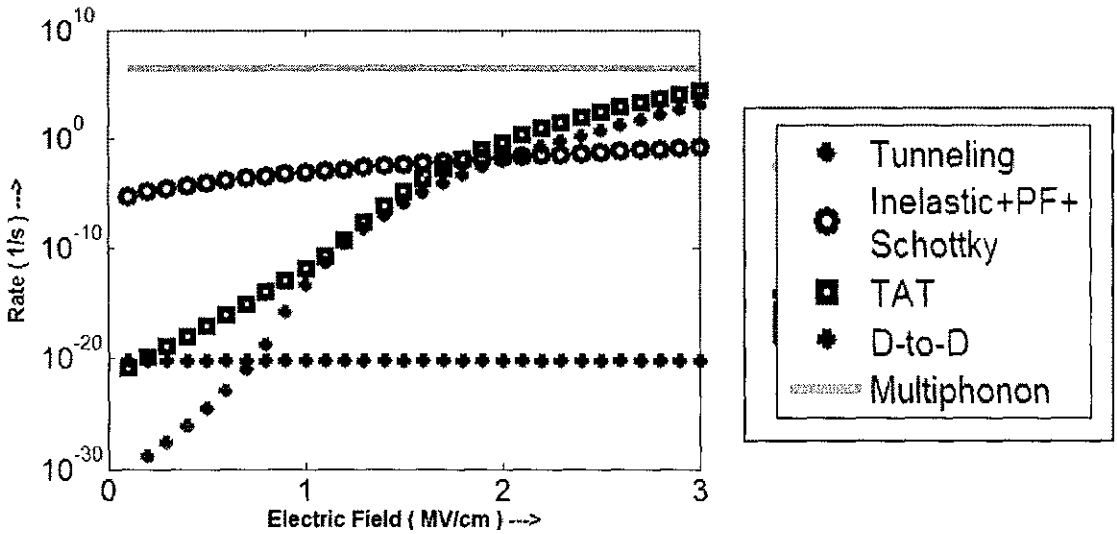


Figure 37: Rates of transport processes.

Fig. 37 shows the rates for the various conduction mechanisms modeled in chapter 3 in a comprehensive manner. A number of features are made obvious by the rates given in Fig. 37. First, it is observed that the rate of multiphonon transition is high compared to other mechanisms such as TAT, TAPF (Tunneling assisted Poole-Frenkel), and FN tunneling at low electric fields. This process if independent of the applied bias, and is the most important component of low field leakage. Furthermore, since it depends on phonons, this rate is expected to become even stronger

at higher temperatures. Thus, these calculations and analyses point towards higher (though relatively flat and constant) leakage currents at low biases and higher temperatures. At high electric fields, the net rate shown (consisting of Poole-Frenkel and inelastic tunneling) will contribute a larger current as discussed later in the section. In particular the Trap-Assisted processes will finally become the dominant mechanism. It may be noted that ultimately, even the Poole-Frenkel mechanism depends on the trap densities, since this process amounts to the emptying of traps that have been filled by electrons. An alternative explanation of the role of a high oxide defect density N_T emerges on the basis of its current contribution [as given in equation (3.21)] in this Cr/HfO_2/Cr scenario.

4.3 ROLE OF TRAPS AND DEFECTS

The importance of traps/defects in oxides on rates of the transport mechanisms has been briefly mentioned in the previous section. This section provides a quantitative comparison of how the trap positions and trap density affect the rate of conduction mechanisms that depend on defects. This provide a better insight into the internal transport physics.

Transport processes such as trap assisted tunneling (TAT), defect to defect transitions, Poole-Frenkel, Inelastic emission and absorption due to multiphonon transitions are noted to depend on traps (both in terms of their energies and densities) in the oxide. Based on the models in section 3.2, in Table 4.2 below we classify the role of trap level/energy and/or defect density on each of the transport mechanisms.

Table 4.2: Processes affected by trap energy and defect density.

Transport Process	Trap Energy	Defect Density
TAT	X	X
D-to-D		X
Inelastic emission	X	
Inelastic absorption	X	
Poole-Frenkel	X	

In HfO_2, trap levels due to oxygen vacancy are identified as the main electrically active sites (Xiong 2078) with trap levels at 0.8eV and 2.1 eV. HfO_2 grown by the atomic layer deposition (ALD) process [62] that have additional defect states based on the precursor used (Lukosius 4381). The films are reported to contain hydrogen, nitrogen and carbon based defects. The interstitial defect levels cause additional energy states in the HfO_2 bandgap. Defect states 0.3 eV below the conduction band of the oxide is formed by interstitial hydrogen. Nitrogen is reported to form interstitial and substitutional defects in the deep level of 3eV to 4 eV below the conduction band. Other impurities and defect related traps are 0.6 eV below the conduction band of the insulator [62]. As in table 4.2, trap assisted tunneling (TAT), Poole-Frenkel, Inelastic emission and absorption processes seem to depend on trap levels. In the following figures the effect of uniform trap levels on the rate of TAT, PF, inelastic emission and absorption is shown.

Comparison based on trap levels

From Fig. 39 and Fig. 40, we can see that increase in trap energy levels lead to increase in rate of defect dependent transport processes predominantly in Poole-Frenkel, TAT, and inelastic absorption via multiphonon process conduction mechanisms

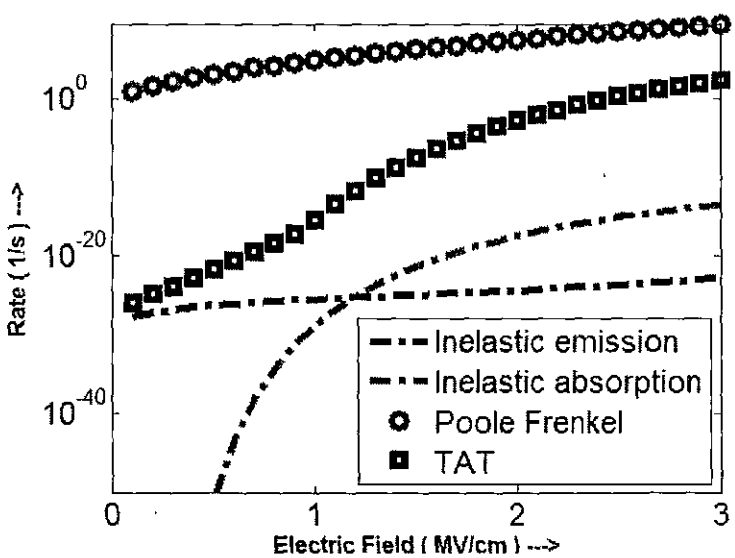


Figure 38: Trap levels 0.8 eV and 2.1 eV.

Reduction in the number of trap energy levels can lead to lesser leakage current, as it will be observed later that TAT and Poole-Frenkel processes significantly contribute to leakage current density.

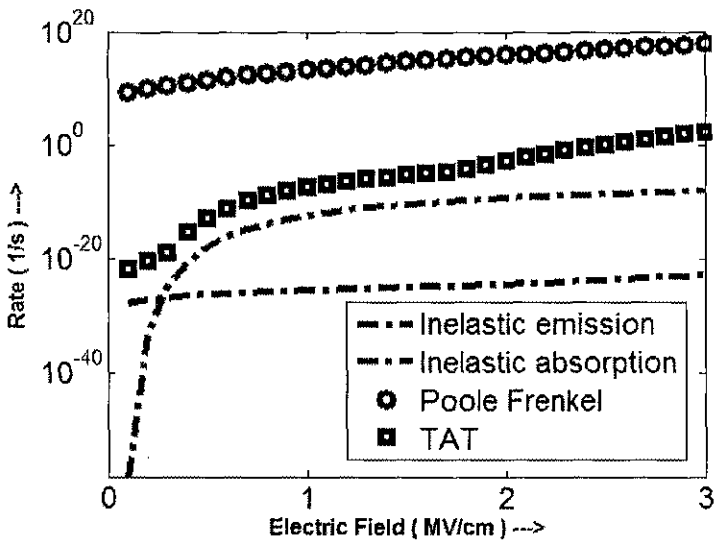


Figure 39: Trap levels 0.3 eV, 0.8 eV, 2.1 eV, and 3 eV.

Comparison Based on Defect Density (With Uniform Trap Levels 0.8eV and 2.1 eV)

The defect density in HfO_2 is known to vary from ~10^{12} cm^{-3} to ~10^{19} cm^{-3} [63]. Intuitively, we can predict that greater the number of defects per unit volume, the higher is rate for processes that depend on traps. From table 4.2, effect of defect density was observed in TAT and defect-to-defect transition processes. The results showing increases in rates of TAT and defect-to-defect processes with enhancements in defect density from 3 x 10^{18} m^{-3} to 3.5x 10^{22} m^{-3} are shown below in Fig. 40 and Fig. 41. In Fig. 40, though the legend shows defect-to-defect transition process, but there are no actual data points seen in the figure. This is because the rate is insignificant and so does not register on the plot, whereas, with increase in defect density, one can view an increase in defect to defect rate as it becomes significant due to the exponential dependence of this process on defect density [refer equation (3.23)].

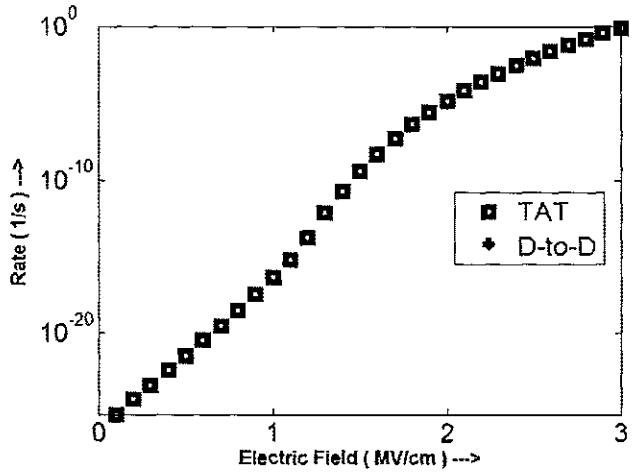


Figure 40: Rate for defect density 3 x 10^{18} m^{-3}.

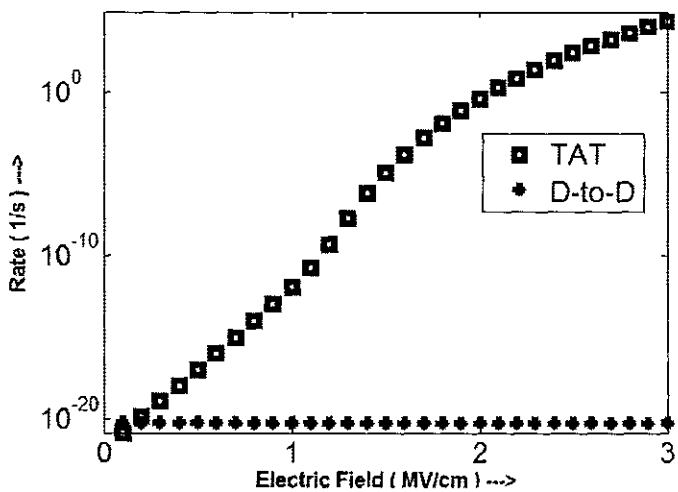


Figure 41: Rate for defect density of 3.5 x 10^{22} m^{-3}.

TAT Based On Trap Distribution

From our model, we could analyze the effect of trap positional distribution (uniform versus delta-function) on transport processes. After the investigation of trap density on processes in the previous section, the trap assisted tunneling (TAT) process was seen to be the prominent process. Here, the role of homogeneous trap positional distributions on this prominent TAT mechanism is analyzed. Fig. 42 below shows the effect of trap spatial distributions. The traps following a delta function profile in the oxide were taken to vary in position along thickness of

oxide. Three specific positions were chosen in this analysis: traps taken to be at the left-side (close to cathode), then traps located at the center, and finally traps to the right (close to anode), for a defect density of 3.5×10^{22} m^2.

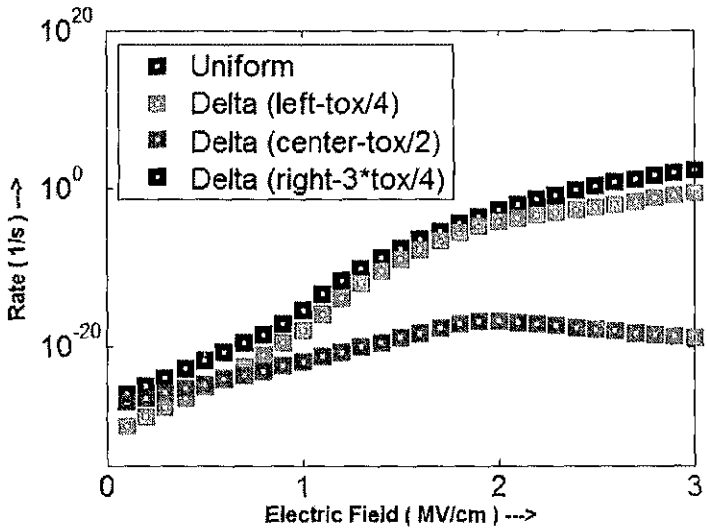


Figure 42: Uniform distribution versus delta-function of traps.

From the above figures, it can be deciphered that the distribution and positions of traps both play a significant role in determining and influencing the TAT rate. The closer the position of traps is to the cathode, the rate of TAT increases as the thickness for the electrons to tunnel into traps from cathode decreases. Note that Fig. 42 does not have data points related to traps positioned near anode as the rates become insignificant. Similarly, uniform distribution of traps show the highest trap assisted tunneling rate as the thickness (i.e., distance) the electrons have to cross is optimally reduced in a collective fashion. The important lesson from the above exercise is that in order to reduce trap-related leakage currents, one should try to eliminate uniformly positioned traps. Small clusters (typically near either ends of the device) might not be as damaging in terms of leakage.

4.5 MODEL VALIDATION

Our model that covers various transport processes was validated with experimental data published [57] for Cr/HfO_2/Cr MIM structure. The parameters extracted from the experiment were used in our model and are listed in Table 4.1. This model allows us to examine the dominant leakage current conduction mechanism in the MIM system under consideration. From Fig. 43, we can conclude that the system we investigated is dominated by current density due to traps.

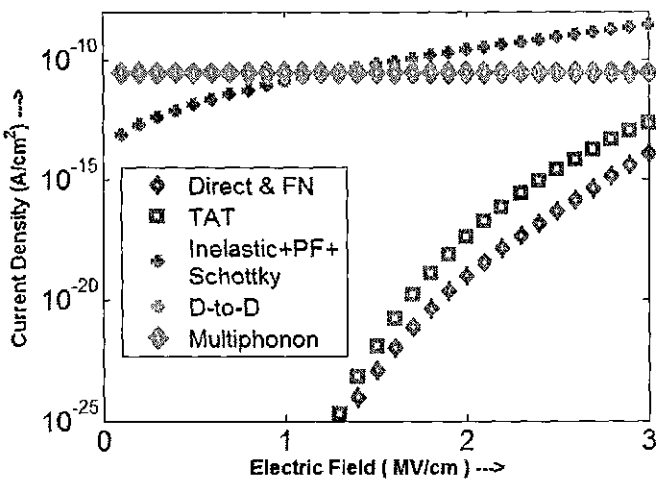


Figure 43: Current density (J) Vs electric field (E) for transport processes in Cr/HfO_2/Cr.

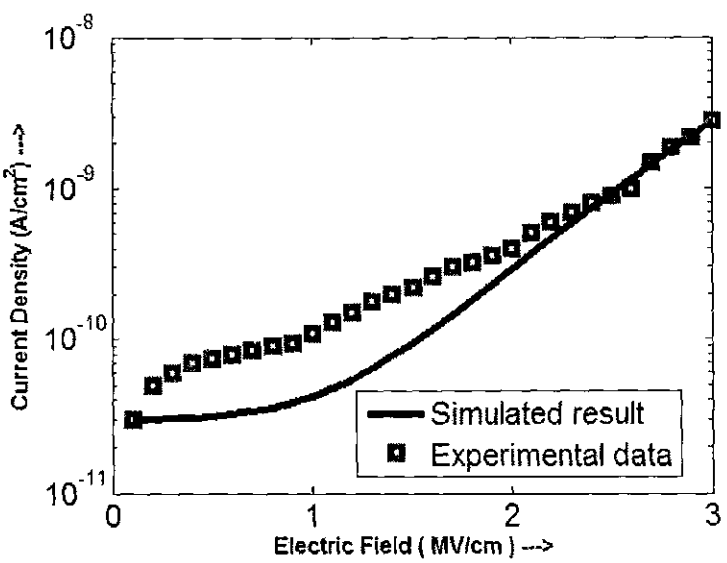


Figure 44: Evaluation of simulated data with experiment for Cr/HfO_2/Cr system.

In Fig. 44, the simulated model is validated with the experiment data [57]. As observed, the simulated data matches the experimental data in the range of 1.5 MV/cm to 3 MV/cm. The difference in current density at fields lower than 1 MV/cm could be due to surface currents that are not included in this model. Also, the experimental data actually shown in Fig. 44 is not very accurate due to human error during extraction from the published paper by El Kamel et al. This occurred since actual numerical values from the El Kamel data were not available.

The aim of this research to predict leakage current density in MIM structures was further accomplished by using another high-k oxide system. The TiN/ZrO_2/TiN system was chosen, with a ZrO_2 thickness of 7 nm and a capacitor area of 1.77 x 10^{-6} m^2 according to available data in the published literature. The experimental data and material parameters (Table 4.3) were extracted from [61] and plotted in Fig. 46.

Table 4.3: Parameters for ZrO_2.

Parameters	**Value**	**Parameters**	**Value**
Permittivity of free space	8.854×10^{-12} F/m	Band gap	5.4 eV
Optical permittivity	5	Barrier height	1.45 eV
$\hbar$	1.054×10^{-34} m^2 kg/s	Trap energy	1.13 eV
Electronic charge	1.6×10^{-19} C	Defect density	3×10^{24} m^{-3}
Electronic mass (me)	9.11×10^{-31} kg	Phonon frequency	1.0×10^{13}
Electronic mass in oxide	$1.2 * m_e$	Huang-Rhys factor	1
$\hbar\omega$ for inelastic multiphonon transitions	0.04 eV	R_{Rid}	1.14×10^{-28}
Boltzmann constant	1.38×10^{-23} m^2 kg/s^2	Number of phonons	1

The current density of Fig. 46 was first broken up into the constituent mechanisms as shown in Fig. 45. Here again, we observe from Fig. 45 that the dominant processes contributing to leakage current are TAT, PF, Schottky, FN, and inelastic tunneling.

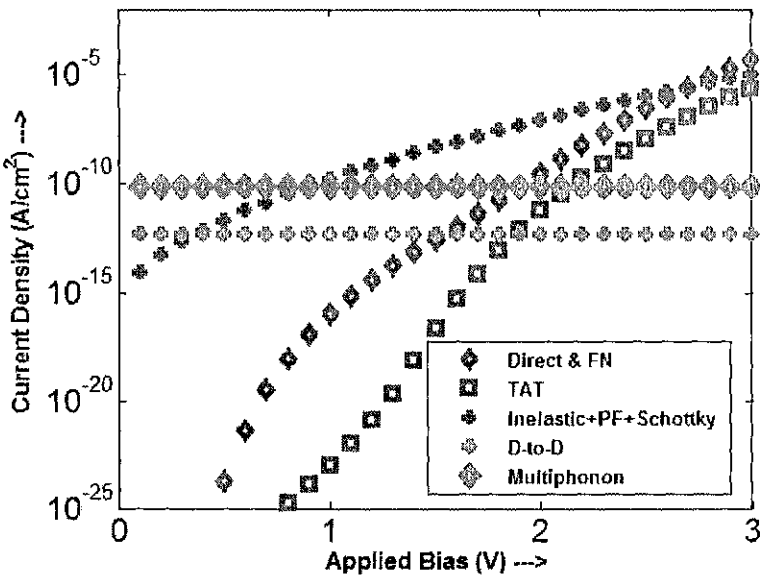


Figure 45: J versus E for transport processes in TiN/ZrO_2/TiN structure.

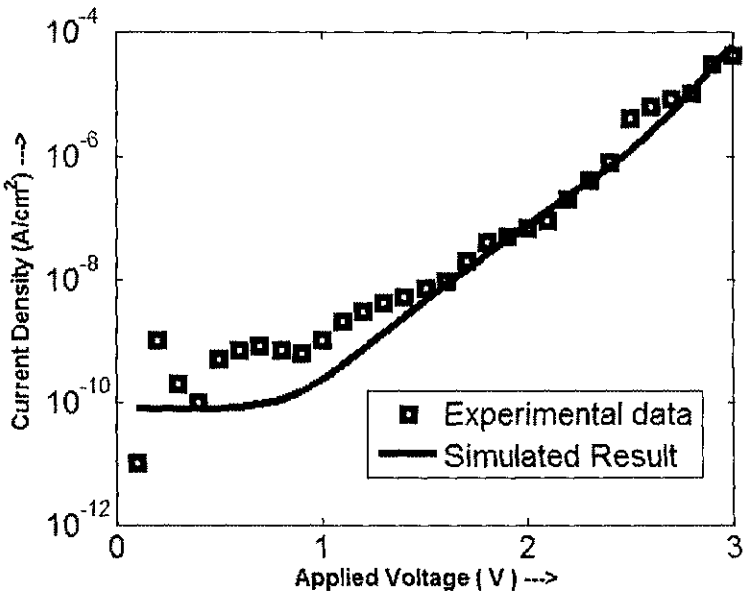


Figure 46: Evaluation of simulated data with experiment for TiN/ZrO_2/TiN system.

Comparing HfO_2 and ZrO_2 system for dominant conduction mechanisms

For the above two systems considered (Figs. 43 and 45), we observe that the dominant mechanisms are TAT, FN tunneling and net current density due to traps that includes Schottky emission, Poole-Frenkel, and inelastic emission and absorption via multiphonon transitions. TAT and FN are more predominant in the $TiN/ZrO_2/TiN$ structure due to the higher defect density and lower barrier height as compared to the $Cr/HfO_2/Cr$ MIM structure. From Figs. 44 & 46, we observe that our model fits very well with the experiment data published in [61].

4.6 MATERIAL PARAMETERS FROM CASTEP

As stated in chapter 3, the material properties used in our simulation are due to the electronic structure of the material and calculated from a quantum mechanics based software program called CASTEP. Our aim was to obtain, compare, and validate the band gap and optical permittivity for HfO_2 obtained from molecular, many-body calculations. Density functional theory (DFT) is one such theoretical approach that enables the evaluation of a range of material parameters based on such molecular-level calculations. However, as with any theory, any DFT approach uses one of several approximations. Results obtained from DFT under any one of the approximations can differ somewhat, so here we actually used CASTEP under different approximations to obtain a variety of results. The objective in doing so was two-fold: (a) To know and appreciate the differences in parameters obtained from the various approximations, and (b) Obtain theoretical predictions for some of the material parameters. In some cases, experimental data on material parameters, especially for the new class of high-k materials is not known. So such values yield a useful starting point. Examples of material parameters that can be obtained from CASTEP include: phonon dispersion characteristics, effective masses, bandstructure including material bandgap, energy-dependent density of states, frequency dependent permittivity including the optical permittivity etc.

Results from the simulation set up for CASTEP, which was described in section 3.7, were obtained. These are presented and discussed next in this section.

(A) Pure Hafnium Oxide Without Vacancies -- Band Gap

Pure Hafnium oxide monoclinic crystal structure was constructed within the CASTEP tool and simulations run based on the sX and the sX-LDA methods to compare the band gap results. The objective was to compare the values obtained from these two methods, and also to evaluate these values with experimental data. The band gap obtained from the simulations with the sX method was 3.047 eV, and with the sX-LDA method it was 4.335 eV. As discussed in section 3.7 the sX-LDA method provides a better approximation for the band gap. The experimentally reported values are roughly around 5.5 eV for HfO_2.

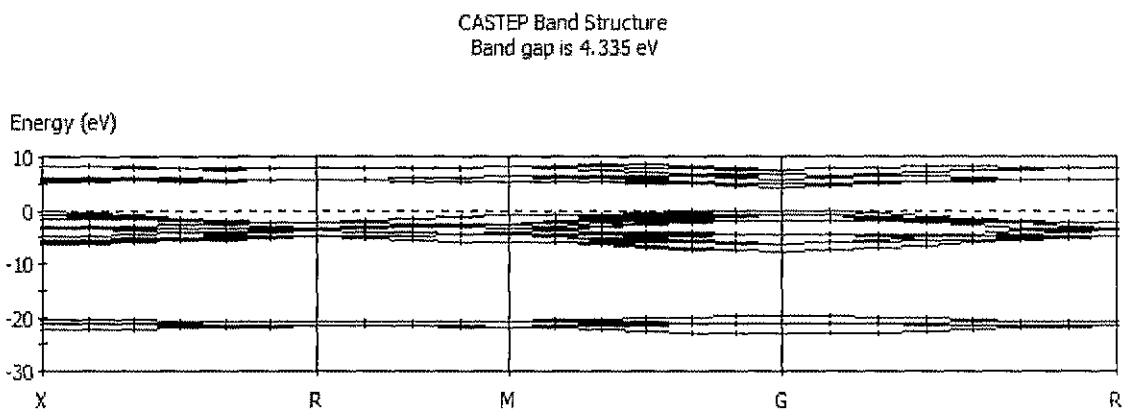


Figure 47: Bandstructure from sX-LDA functional in CASTEP for HfO_2 without vacancy.

The band gaps obtained from the two above-mentioned methods can also be compared to the value from an LDA method published in [64]. The uncorrected LDA band gap value was reported to be 3.4 eV which is much lower than that from the sX-LDA method. Hence, using the sX-LDA method within CASTEP is a superior alternative and yields material bandgap that is better than some of the recent results in the literature.

(B) Comparison of Bandgap For HfO_2 With Vacancy Sites

Having determined that the sX-LDA method is a better approximation and can provide more accurate numerical results, simulations for HfO_2 were next set up with a vacancy. This was driven by the known presence of oxygen vacancies that have been determined experimentally. Such vacancy defects are common in many of the emerging high-k materials for which the process technology has not yet fully matured. The band gap was obtained to be 1.962 eV under this condition of an oxygen vacancy. This suggests that defect states are introduced in the band gap, thereby reducing the band gap value. This observation was determined by plotting the total density of states for pure HfO_2 and HfO_2 with vacancy, as shown in Fig. 48 and Fig. 49. The simulation of HfO_2 with vacancy in Fig. 49 clearly shows states introduced in the band gap. In this figure, the Fermi level is taken to be at the reference level, as marked by a 0 on the figures below.

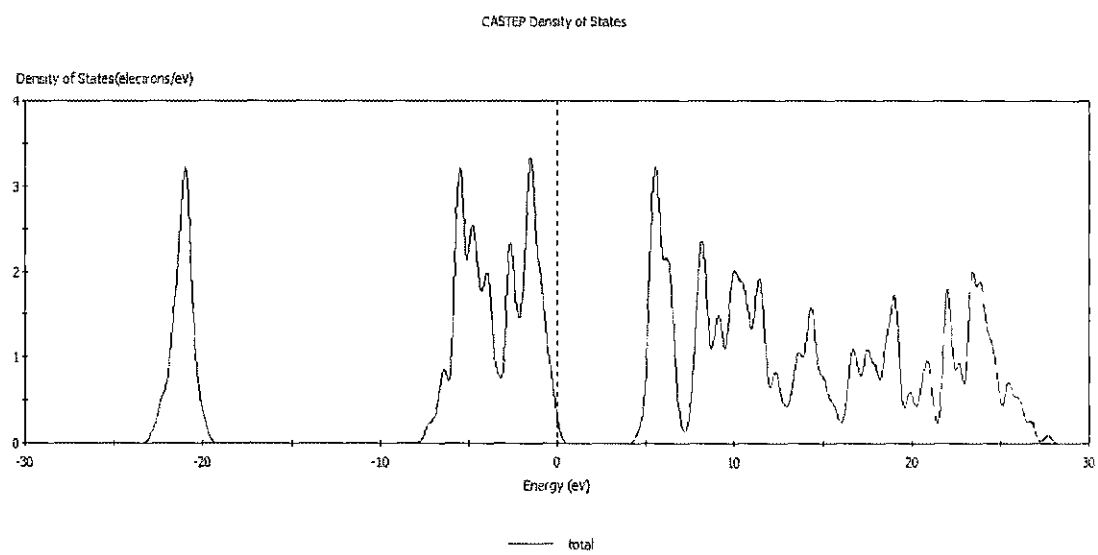


Figure 48: Density of states from the sX-LDA functional using the CASTEP software tool for HfO_2 without vacancy.

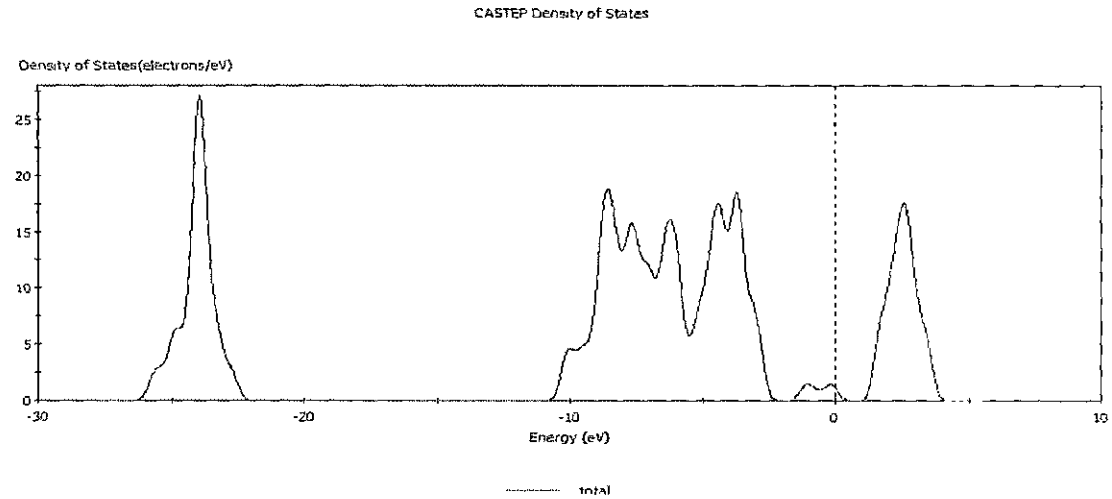


Figure 49: Density of states from the sX-LDA functional using the CASTEP software tool for HfO_2 with an oxygen vacancy in the lattice structure.

(C) Use of the Generalized Gradient Approximation (GGA) Functional

Another important material property that was observed using the above methods was the optical permittivity. An evaluation of this parameter was deliberately carried out, since the Poole-Frenkel conduction does depend on the optical permittivity parameter. Hence, an independent determination from a materials standpoint serves as a useful task. In this study however, the sX-LDA method was not used within CASTEP. This was because the CASTEP output file clearly stated that optical permittivity obtained from the non-local functional i.e., sX-LDA method can be inaccurate. Therefore, the simulation was set up to run with the GGA method. However, for completeness, the bandstructure and density of states were also computed for HfO_2 on the basis of the GGA method. The results from this simulation are presented in Fig. 50 (a) and 50(b) and Fig. 51.

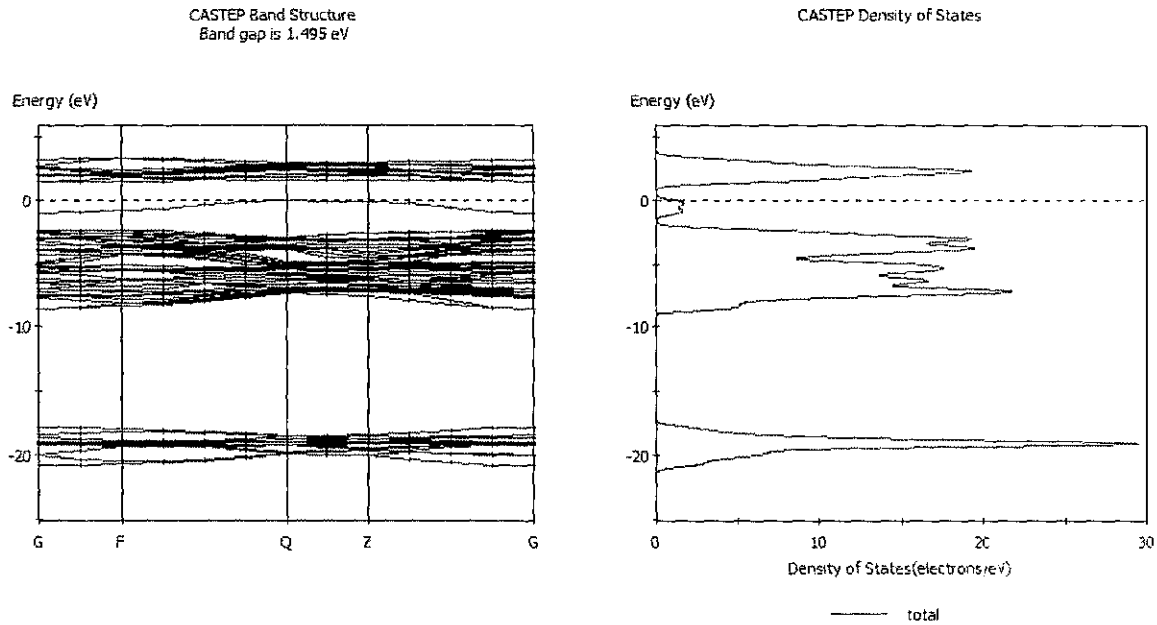


Figure 50: (a) Bandstructure for HfO_2 with vacancy, and (b) Density of states obtained from CASTEP for HfO_2 with vacancy.

(D) Optical Permittivity Results

It is clearly seen that the band gap is underestimated by the GGA method (1.495 eV) for HfO_2 with vacancy, as compared to the results of 1.962 eV obtained on the basis of the sX-LDA functional. Also, it was noted that the optical permittivity from GGA method in Fig. 51 was about 4.3. This optical permittivity is very close to the value reported from LDA functional with an optical permittivity of 4 [64]. It is also close to the reported experimental values. Therefore, the material parameters used in our simulation is based on numerical simulations from CASTEP and other experimental data as appropriately referenced.

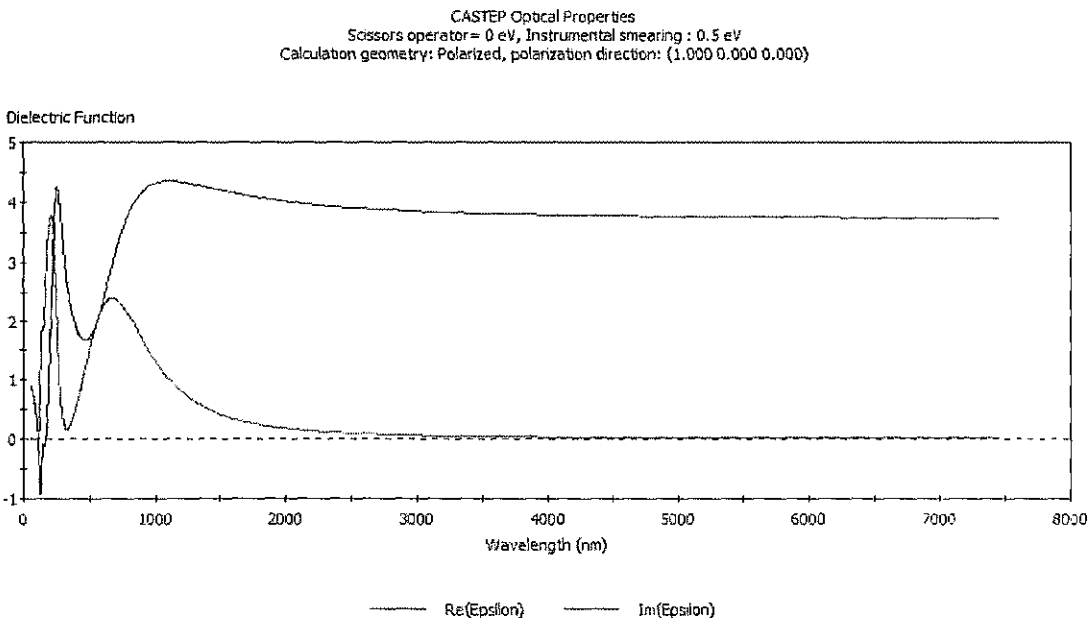


Figure 51: Optical permittivity as obtained from the GGA method using the CASTEP tool.

CHAPTER 5

CONCLUSION AND FUTURE WORK

5.1 CONCLUSION

Numerical simulation models were developed to determine the leakage current density in high-*k* dielectric materials due to an externally applied bias in a Metal-Insulator-Metal structure. The goal to incorporate the carrier transitions in and out of traps to provide a complete transport picture in Metal-Insulator-Metal structures was accomplished. We acquired in-house capabilities for simulating leakage current density in user specified high-*k* materials in MIM structures and to validate experimental measurements. Another crucial objective was to assess the relative importance of each transport process and its electric-field dependence to determine dominant current conduction mechanisms. These objectives were successfully achieved. For purposes of demonstration, we investigated HfO_2 as the high-*k* material/insulator for an MIM structure in detail, and also validated the model for leakage current density in ZrO_2. Various transport processes were used to obtain the best fit for experimental data to determine the leakage current density and its underlying conduction mechanisms.

The model development was initiated by considering individual transport processes that contribute to current conduction in high-*k* material. To demonstrate, each process was discussed in detail in chapter 3, and the rates from these mechanisms were presented in chapter 4 for 10nm thickness HfO_2 MIM structure. The rates from these processes helped in focusing on dominant mechanisms such as TAT, Poole Frenkel, Schottky Emission, direct and FN tunneling (which is more pronounced in lower oxide thickness). Observing that traps and defect densities play an important role in leakage current density, process dependent on traps were examined. In order to complete the transport picture, trap dependent processes were combined to obtain current density in the steady state. This model included processes that injected carriers into traps and process taking out carriers from traps to contribute to current, thereby completing the current transport

picture. To determine the dominant current conduction mechanism, various transport processes were simulated for HfO_2 and ZrO_2 which are materials known to have higher defect densities than the conventional SiO_2 oxide. As expected, the trap dependent process proved to be a dominant mechanism for leakage currents. Effects of location and distribution of traps in oxide were also studied. The effectiveness of this model was tested and compared with experimental data for HfO_2 and ZrO_2.

The parameters such as dielectric constant and band gap, used in the simulation of current density in HfO_2 were obtained from CASTEP, a tool that uses DFT to extract material properties. These parameters compared well with other research studies and experimental reports. Other relevant material parameters that were used were derived from references that contained the experimental data for the relevant material under consideration. The leakage current density simulated from both these materials compared well with experimental data and the parameters used in the simulation were validated to be physically consistent. Among the various mechanisms, Poole-Frenkel was seen to dominate at higher electric fields. Since this does depend on the occurrence of traps and their specific energies, one can hope to reduce leakage and hope for better outcomes as processing technology is improved in the future. This would also favorably impact the trap-assisted leakage processes.

Finally, molecular level DFT calculations were carried out. An important finding was that a band of energy states with a finite density of states can exit within the HfO_2 material bandgap. This could lead to transport within the high-*k* oxide through such sub-bandgap states and increase the leakage current. These kinds of sub-bandgap transport phenomena were not studied here, but remain a possibility for future research. Also, in comparison to experimental data, the data at lower biases were found to be higher than the theoretical predictions. It is quite possible that such additional sub-bandgap transport could account for the discrepancy at low fields.

5.2 FUTURE WORK

The current transport model developed for predicting the leakage current density and its under lying mechanism at different applied voltage in high-k materials used in semiconductor devices is very useful and generally agreed well with experimental data as discussed above. However, this model can further be improved and the methodology can be applied to different applications. A few such tasks and applications for possible future work are presented below.

1. Leakage current density experimental data that was used to compare with simulated data show variations at the lower fields below 1 MV/cm. Such variations could have occurred due to flash currents, surface currents, relaxation currents or charge trapping. These phenomena could be included in the model to observe their effects on leakage current density.

2. A second possibility might be that the parameters such as the barrier height, and trap energy levels are all uniform and constant for the MIM system. However, due to local variation (e.g., during processing), it is possible that lateral variability might exist. For instance, the barrier height may fluctuate about a mean value along the lateral direction. Consequently, current injection might not be uniform. More seriously, however, since the current injection usually depends exponentially on the barrier height, any fluctuation about a mean value can actually lead to much higher current injection values. Such an occurrence might bring the experimental values more in line with the theoretical predictions. However, detailed calculations, including determination of the mean barrier height and the root-mean-square value of the fluctuations need to be determined.

3. Various processes included in our model can simultaneously occur in a 3D MIM structure. Such competing transport channels can be accounted for by using kinetic Monte Carlo algorithm. Monte Carlo is very general stochastic-probabilistic numerical

method that can be applied to various classes of computational problems in different fields. The method involves stochastic techniques that use random numbers and probability statistics to investigate problems and generate mean values that follow a governing distribution or mathematical model. This technique is employed in everything from economics to physics, to regulating flow of traffic, although the distributions or the mathematic models can vary in each of these cases. The rates from conduction mechanisms are the inputs to the kMC algorithm and the method itself cannot predict these rates. The rates govern the time-dependent evolution of the system, and depend on the conditions of every specific problem.

The algorithm involves the concept of statistically choosing a particular transition process from the set of transport process with rates defined as above during any given time interval. This can be done in a stochastic fashion by choosing appropriate random numbers and using them to select the transition and times from all applicable processes that correctly weigh the occurrences. The kMC algorithm proposed by Gillespie [56] and adopted in [3] can be used to simulate the time evolution of our current transport system. It is written as follows:

(i) The simulation time is initialized to $t = 0$ by specifying an arbitrary electron distribution at the cathode. The energies of the various electrons are chosen to mirror the Maxwellian distribution at the cathode.

(ii) The list of all possible single electron transitions S_j and their individual rates R_j (defined in section 3.2) is formed.

(iii) The cumulative transition rate $R_{tot} = \sum_{j=1}^{N} R_j$ is calculated where N is the number of possible transition processes.

(iv) The transition probabilities are computed by normalizing the corresponding rate against the cumulative rate R_{tot} calculated above. The normalized ratio R_j/R_{tot} then yields the relative weight (or frequency of occurrence) of process S_j.

(v) A random number r_1 from a uniform distribution $r_1 \epsilon (0, 1]$ is generated.

(vi) Using the random number generated in step 5, an appropriate transition process S_j is picked according to the index j given as: $\sum_1^{j-1} R_j < r_j < \sum_1^j R_j$.

(vii) Employing standard Monte Carlo sampling technique, the time increment, i.e., the time that the system stays in that state is computed by generation of another random number r_2 from a uniform distribution as $t_j = -Ln(r_2)/R_{tot}$.

(viii) The time step is updated $t = t + t_j$ and returns to step 5 if recalculation of all rates is not required.

(ix) The simulation is allowed to run until steady state is reached and leakage current density is calculated using equation (5.1) by counting the electrons reaching the anode (say, M) after a desired simulation time (t_{tot}).

$$J_{tot} = \frac{M*q}{A*t_{tot}} \tag{5.1}$$

This algorithm stated above is only a stochastic procedure and the physics involved in determining the leakage current is encapsulated in the quantum mechanical rate models in section 3.2. It does not give an exact result for one, or even a few electrons, but by running the simulation for a large number of electrons the overall average behavior will indeed be reflective of the on-going physics as governed by the various inherent process rates.

4. The effect of space charge, currently excluded in our model, can be added to encompass a wider range of materials and scenarios that can be simulated. This would make the internal electric fields somewhat dynamic and alter the local currents somewhat.

5. An important parameter on which various material parameters depend in semiconductors is the temperature. The effects of temperature on current mechanisms and eventually on leakage current density can be observed and compared to experimental data as a next potential step.

6. Although MIM structures form a critical component in storage, the leakage current mechanisms in transistors (MOS structures) that are the fundamentals of integrated circuits can be studied by modifying the models. Apart from MIM and MOS structures, models can be developed to study leakage currents in other semiconductor devices such as HFETs, MEMS devices etc.

7. Finally, molecular level DFT calculations were carried out. An important finding was that a band of energy states with a finite density of states can exit within the HfO_2 material bandgap. This could lead to transport within the high-k oxide through such sub-bandgap states and increase the leakage current. These kinds of sub-bandgap transport phenomena were not studied here, but remain a possibility for future research. It is quite possible that such additional sub-bandgap transport could account for the discrepancy at low fields between the predictions obtained here and experimental data.

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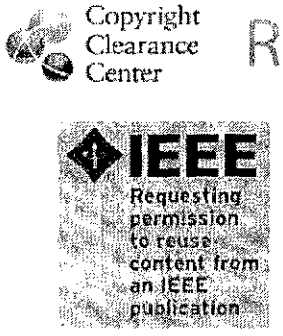

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VITA

NAME: Priyamvada Maleeswaran

DEGREES:

- Bachelor of Science (Electrical Engineering),

  Old Dominion University, Norfolk, Virginia, December 2010.

- Master of Science (Electrical & Computer Engineering),

  Old Dominion University, Norfolk, Virginia, December 2012.